

1. Schematic Page Description :

ZHS/BTM-origins Schematic Ver :

- | | |
|---------------------------------|---------------------------------|
| 01 -- Sch Page description | 21 -- WIFI/BT(NGFF)/Video Codec |
| 02 -- Block Diagram | 22 -- eMMC |
| 03 -- Valley 1/9 (DDRA) | 23 -- TPM /LED |
| 04 -- Valley 2/9 (DDRB) | 24 -- DB /Thermal sensor |
| 05 -- Valley 3/9 (Display) | 25 -- Audio Codec |
| 06 -- Valley 4/9 (SD/PCIE/SATA) | 26 -- USB3/Charger/Hole |
| 07 -- Valley 5/9 (SPI/GPIO/CLK) | 27 -- KB/TP/HW RST |
| 08 -- Valley 6/9 (USB/LPC/I2C) | 28 -- KBC |
| 09 -- Valley 7/9 (Power 1) | 29 -- Charger (BQ24715RGRR) |
| 10 -- Valley 8/9 (Power 2) | 30 -- SYSTEM 5V/3V (MPS670/671) |
| 11 -- Valley 9/9 (GND) | 31 -- Load Switch |
| 12 -- BTM XDP & APS | 32 -- DDR 1.35V(TPS51216) |
| 13 -- DDR3L MEMORY DOWNx16 CHA | 33 -- +1.05V/+1V(TPS54318) |
| 14 -- DDR3L MEMORY DOWNx16 CHB | 34 -- +VCC_CORE(ISL95833) |
| 15 -- Level Shifter (SOC_EC) | 35 -- LDO-1 (G9661) |
| 16 -- Level Shifter (SOC_DEV) | 36 -- LDO-2 (G9661) |
| 17 -- SDIO CardReader | 37 -- Thermal protect |
| 18 -- LCD/CCD/DMIC | 38 -- Power Sequence |
| 19 -- Google Debug | 39 -- SMBUS/I2C |
| 20 -- HDMI | 40 -- BTM PWR TREE |
| | 41 -- Change List |

I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

SMBus table

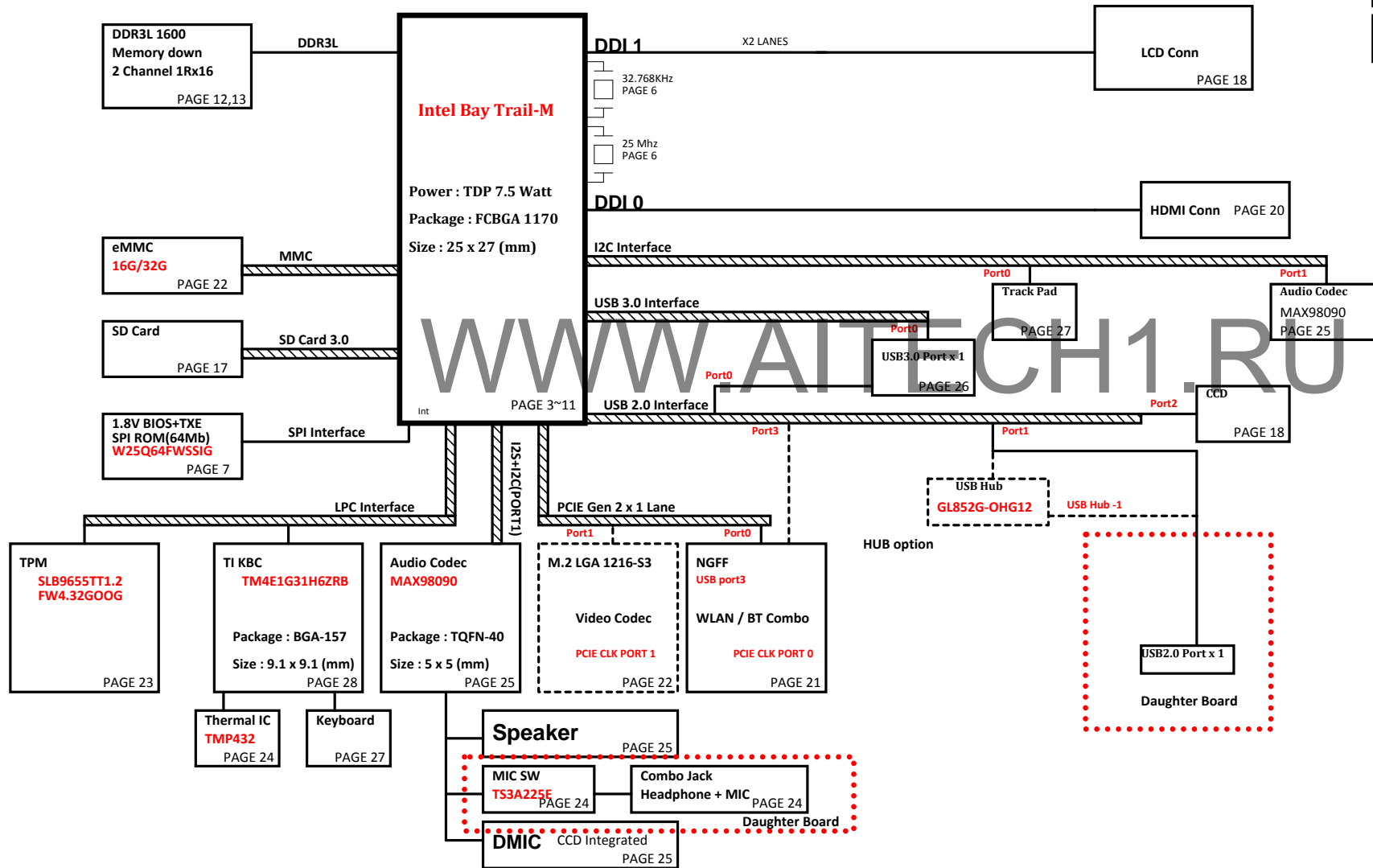
Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

ZHR/BTM-Origins

Intel Bay Trail-M Platform Block Diagram

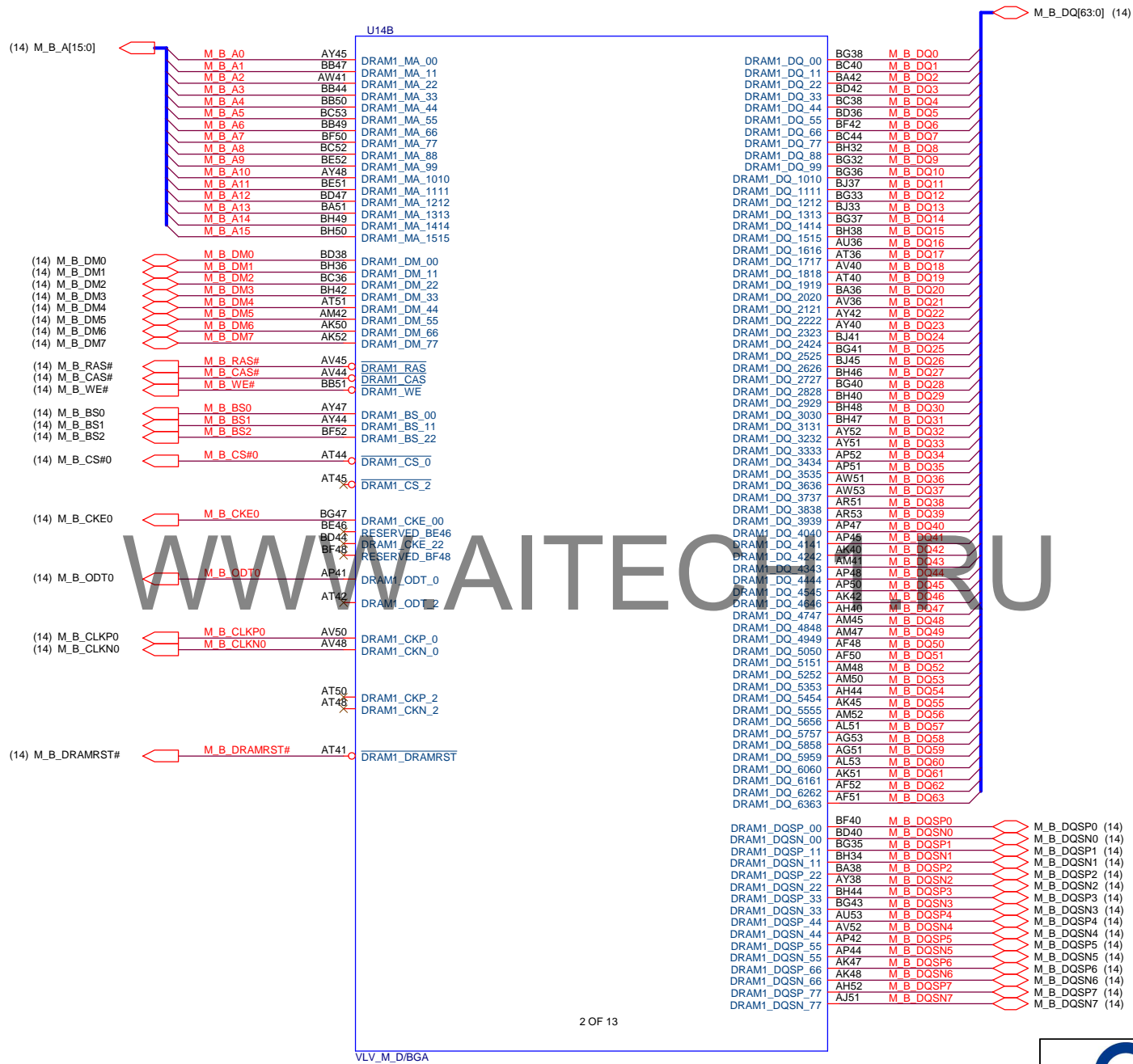
SKUA DC N2820
AJSR1SGUT03 --CPU(1170P)N2820 2.13G SR1SG(FCBGA)STNBSQ



BQ24715 Battery Charger	TPS51216 PP1350
TPS51225 PP3300_DSW/PP5000	NB671GQ-Z PP1000_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	Thermal Protection Discharger

BOM value option:
SX@ => SOiX
NSX@=>none SOiX
HUB@=>USB HUB
3G@ => LTE
GD@ =>Google debug

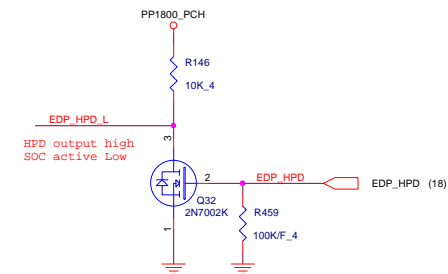
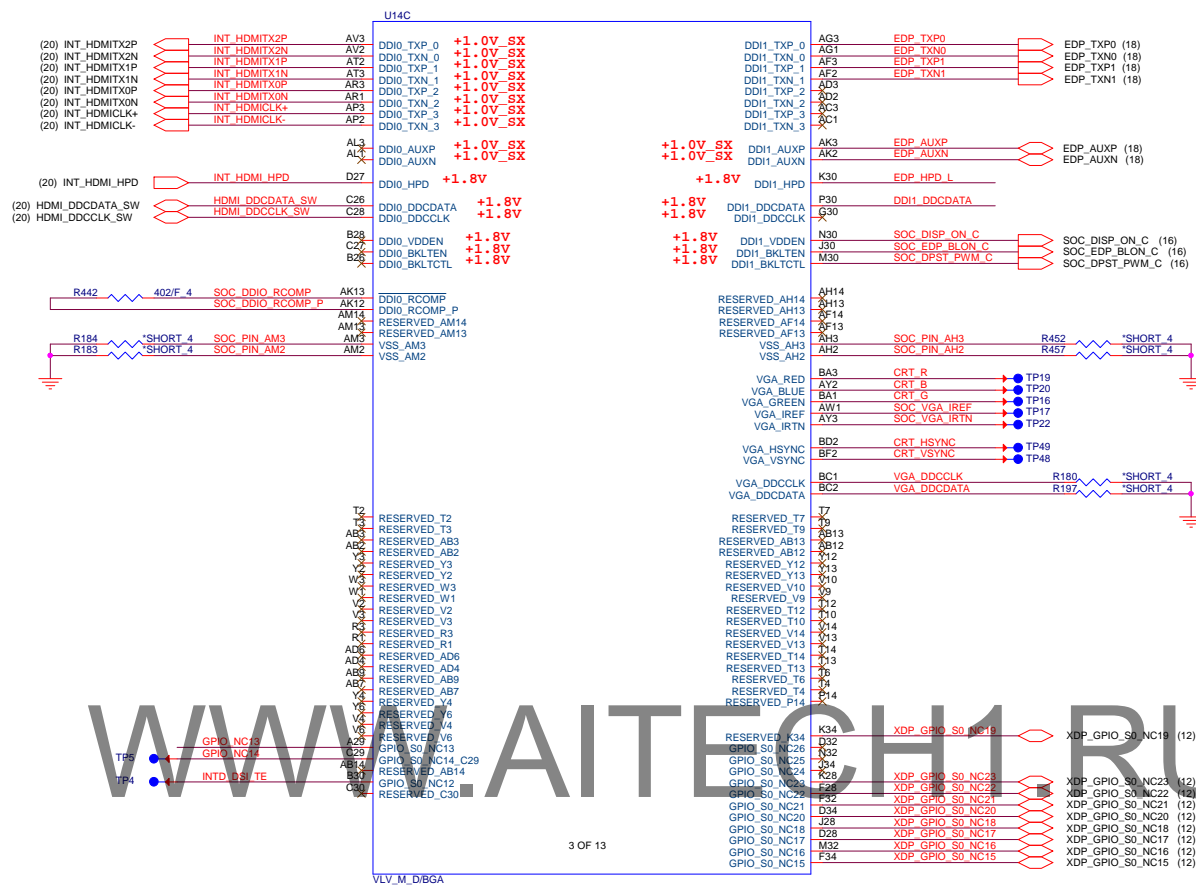




Quanta Computer Inc.

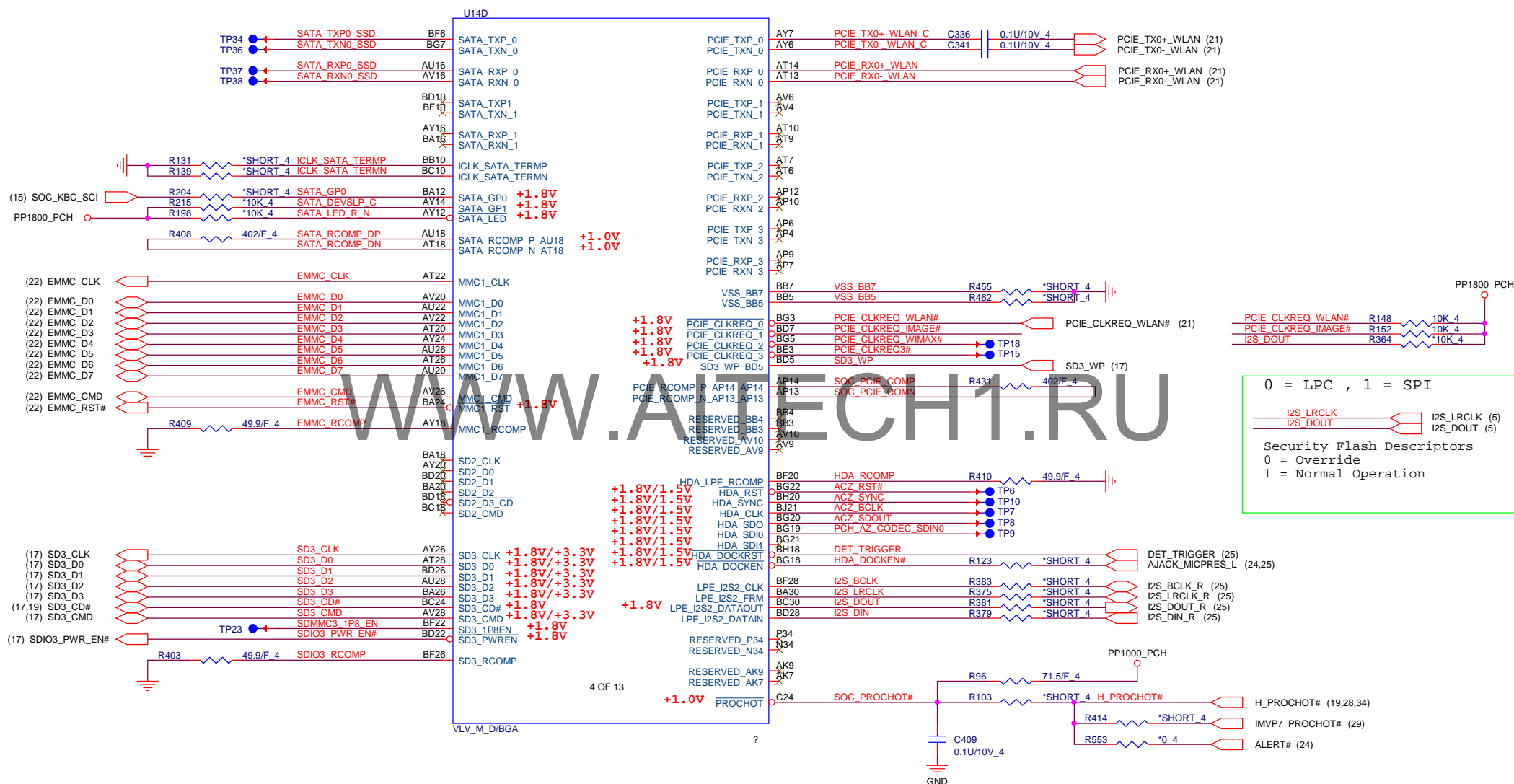
PROJECT : ZHS

Size	Document Number	Rev
	Valley 2/9 (DDR8)	1A
Date:	Monday, August 10, 2015	Sheet 4 of 42

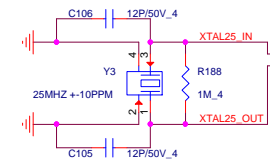


BTM Strapping Table

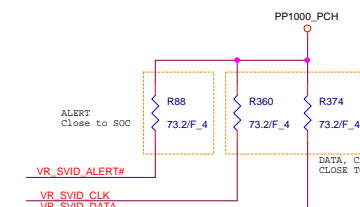
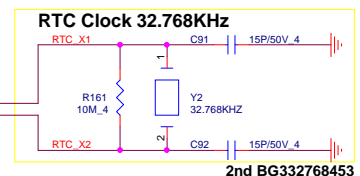
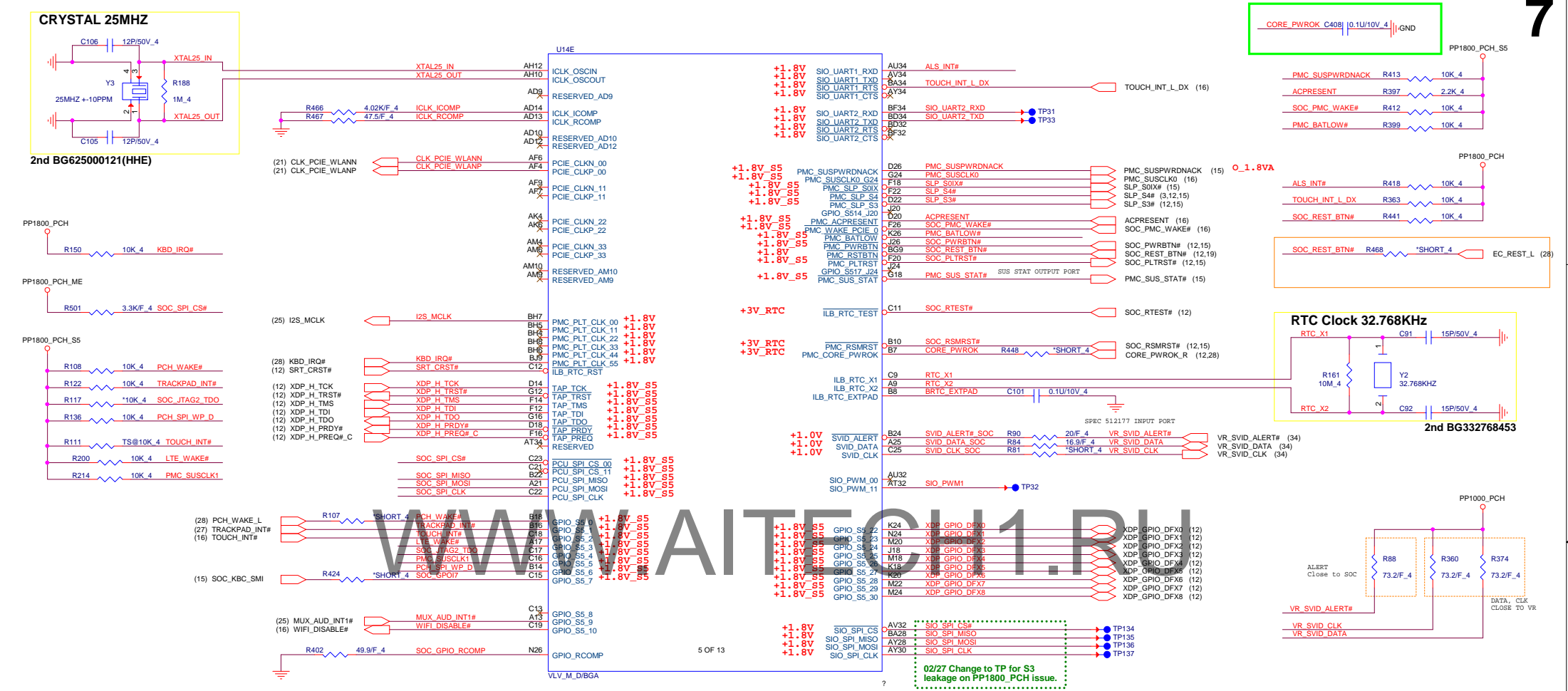
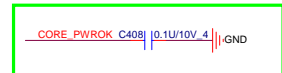
Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	(8) GPIO_SO_SC_56 using SoC internal PU
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	(6) I2S_LRCLK using SoC internal PU
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	(6) I2S_DOUT (28) SOC_OVERRIDE# Q6 2N7002K
DDIO_DDCDATA	DDIO Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	using SoC internal PU
GPIO_SO_NC_13				



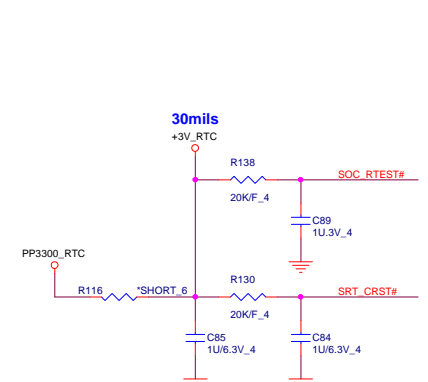
CRYSTAL 25MHZ



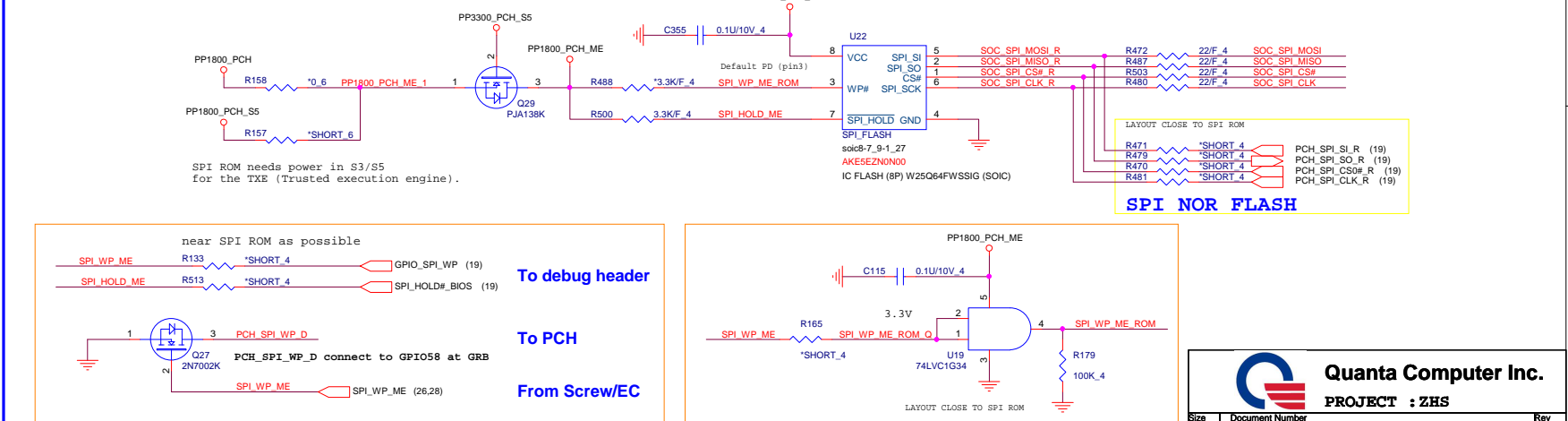
2nd BG625000121(HHE)



RTC Circuitry(RTC)

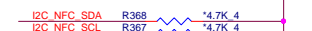
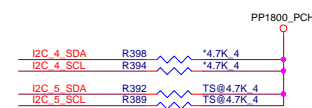
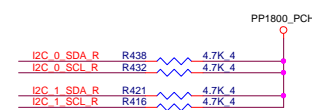
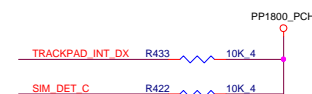
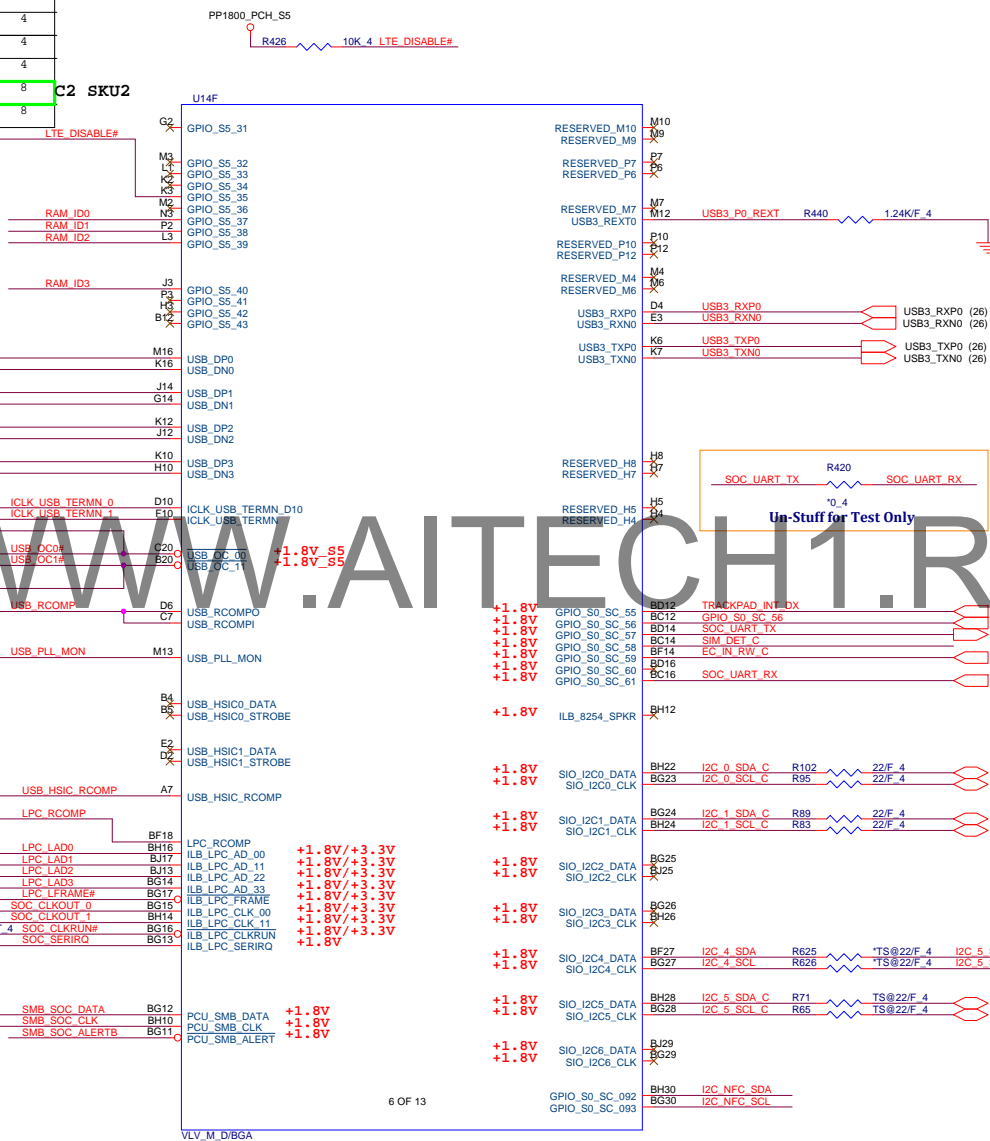
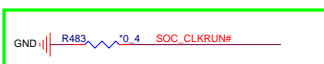
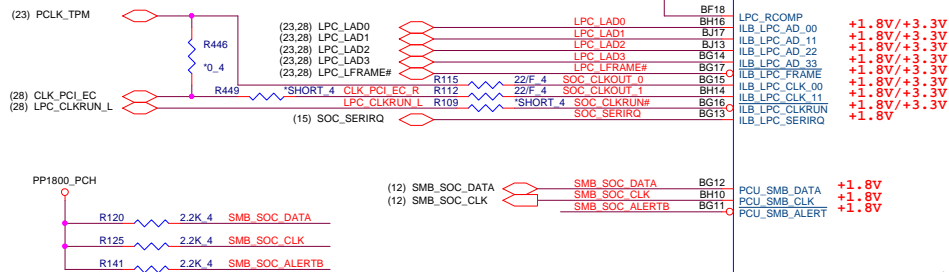
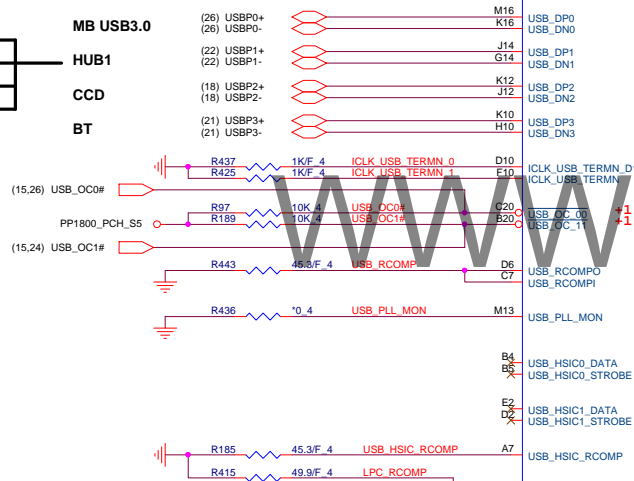
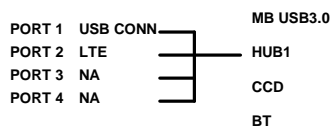
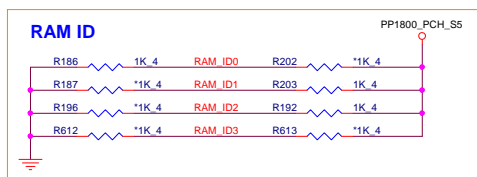


SPI_FLASH

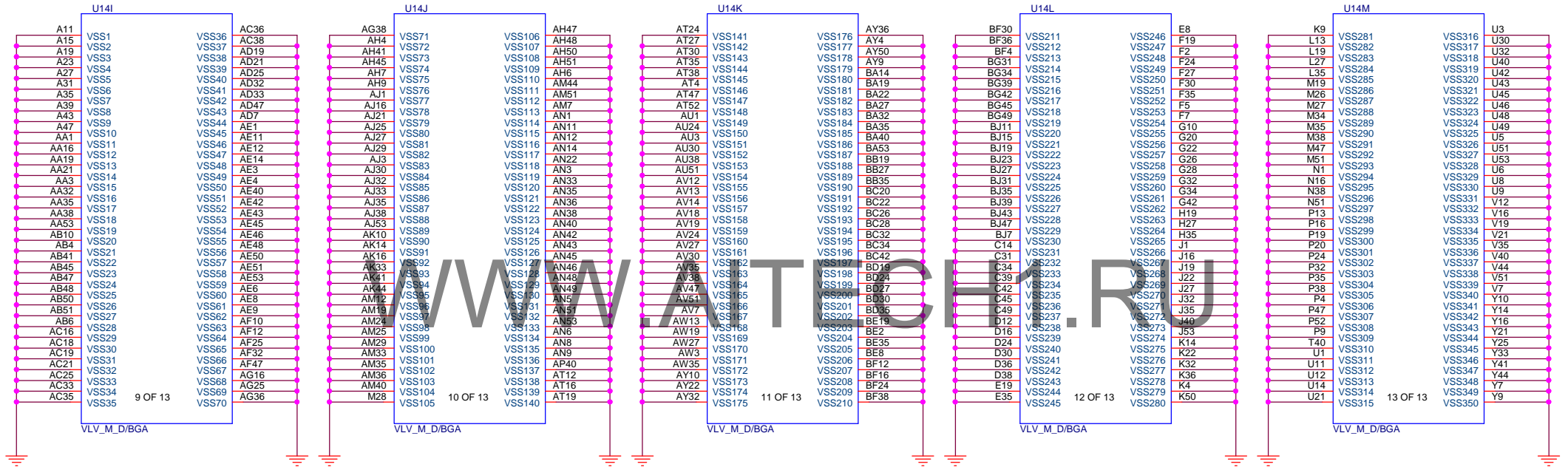


5/19 Update RAM ID for ZHQ and ZHS use.

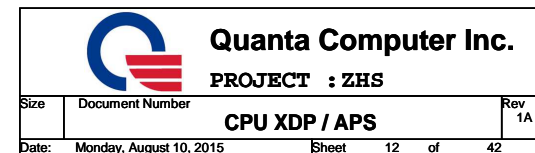
Vender	RAM_ID 210	Q P/N	Mfr. PN	Freq.	Size	Pice
Samsang	0x000	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	4GB	8
Hynix	0x001	AKD5JGETW04	H5TC4G63APF-PBA	1600MHz	4GB	8
Micron	0x010	AKD5DGLSTL07	MT4K128M16JT-125M-K	1600MHz	2GB	8
Hynix	0x011	AKD5PGSTW03	H5TC4G63MFP-PBA	1600MHz	2GB	4
Hynix	0x100	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	2GB	4
Hynix	0x101	AKD5JGETW04	H5TC4G63APF-PBA	1600MHz	2GB	4
Hynix	0x110	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4GB	8
Hynix	0x111	AKD5PGSTW03	H5TC4G63MFP-PBA	1600MHz	4GB	8

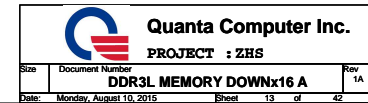






12





<DDR>

BYTE16_23

BYTE24_31

BYTE0_7

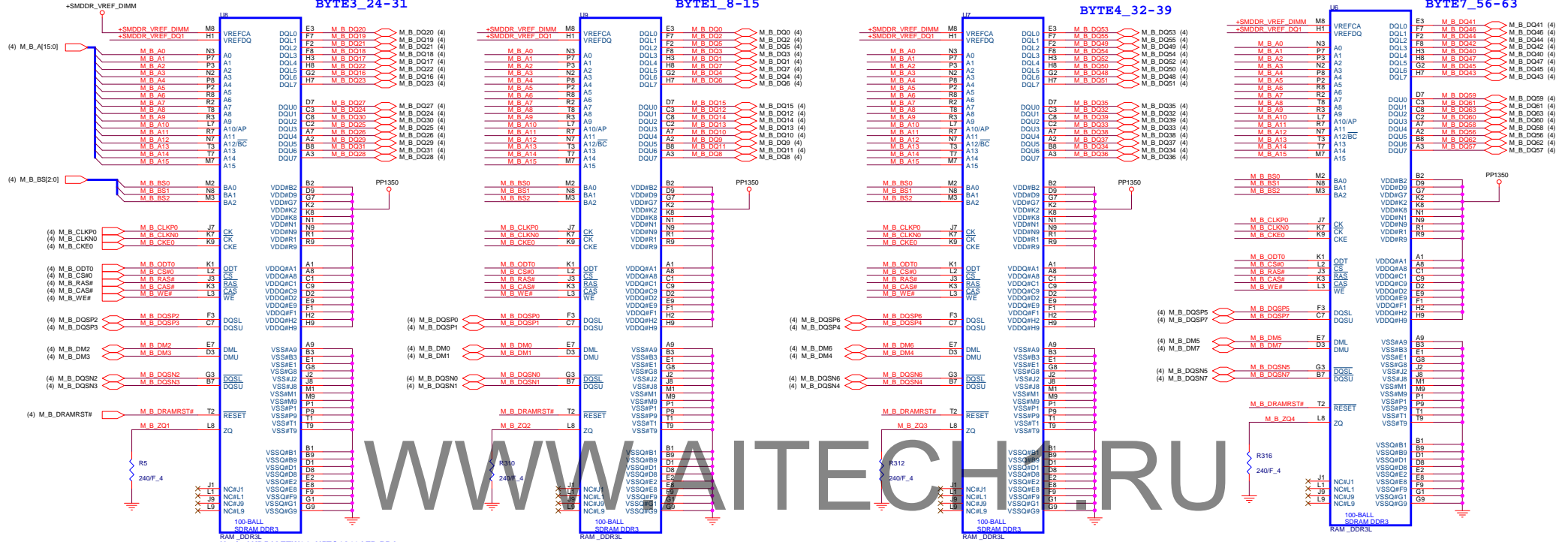
BYTE8_15

BYTE6_48-55

BYTE4_32-39

BYTE5_40-47

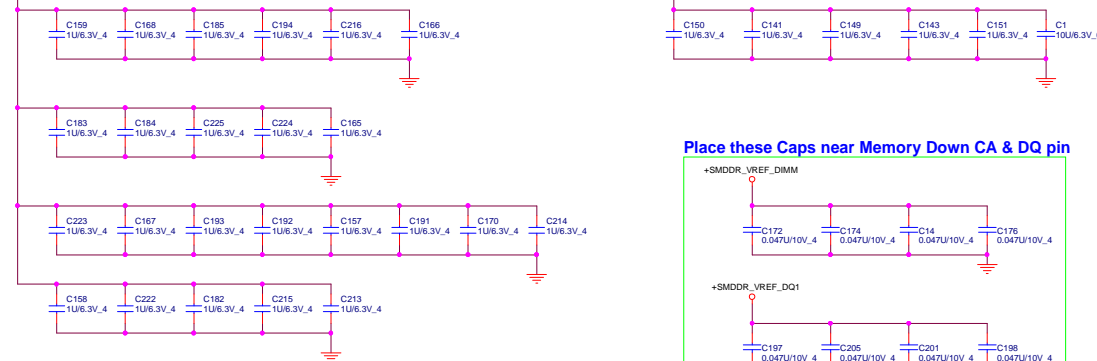
BYTE7_56-63



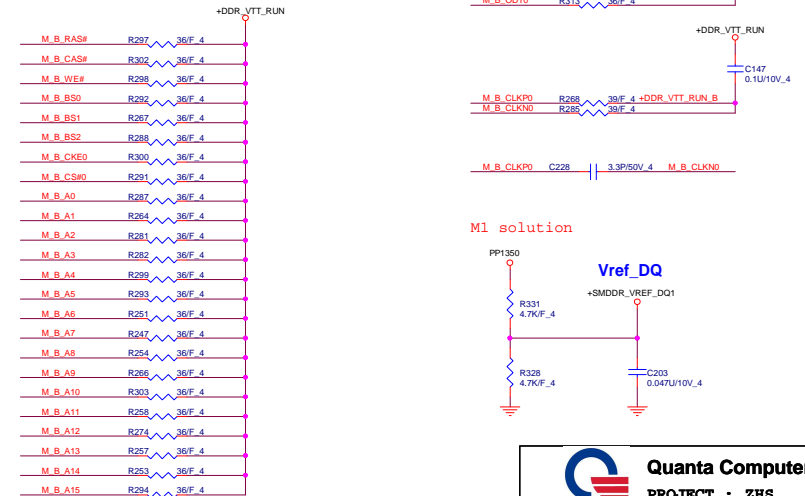
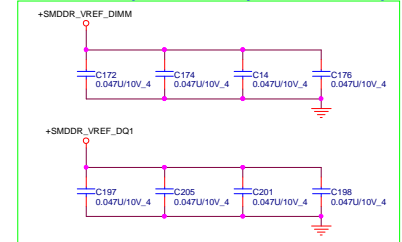
Hynix AKD5JGETW04-H5TC4G63AFR-PBA

Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600MHz 4Gb
Elpida	AKD5JGST400	DDR3L 1333MHz 4Gb
	AKD5JGST404	DDR3L 1333MHz 4Gb

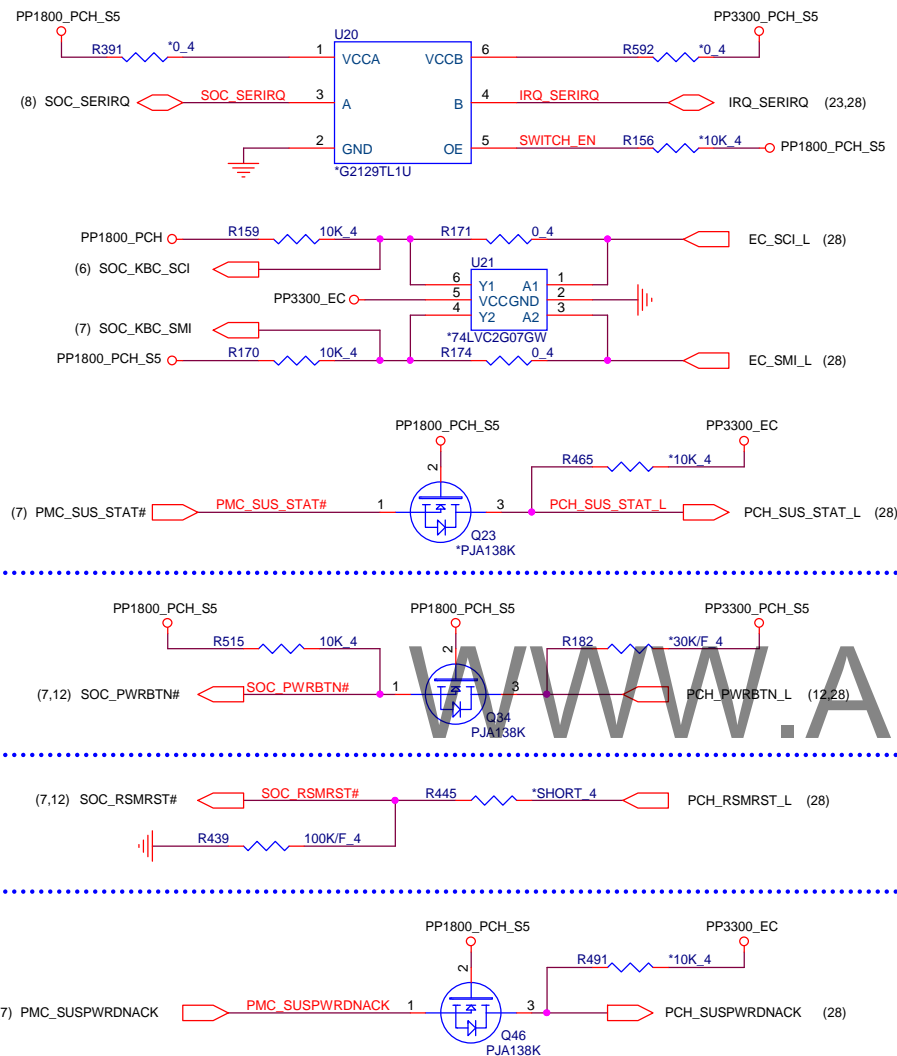
Place these Caps near each X16 Memory Down



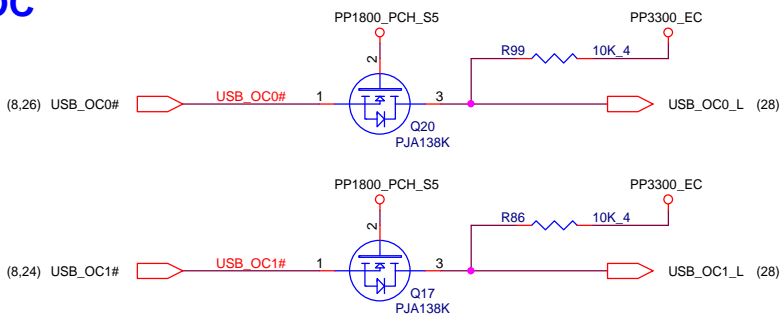
Place these Caps near Memory Down CA & DQ pin



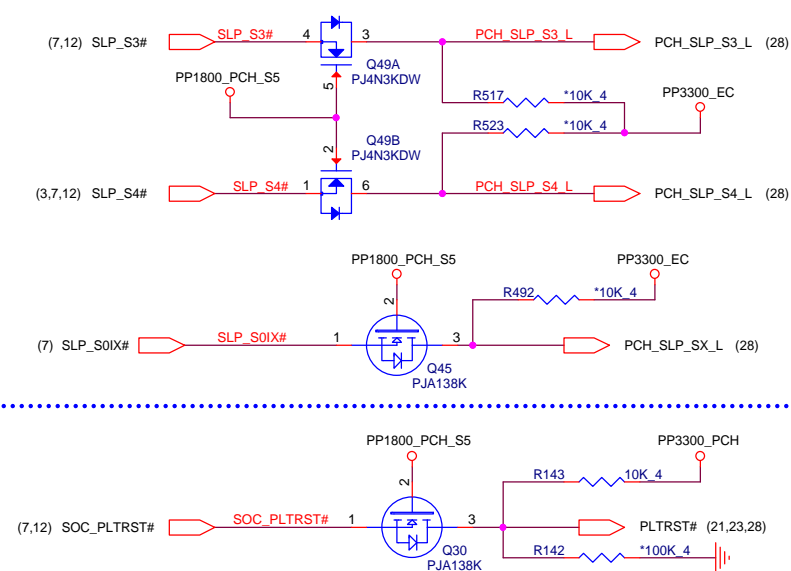
PWRON SEQUENCE



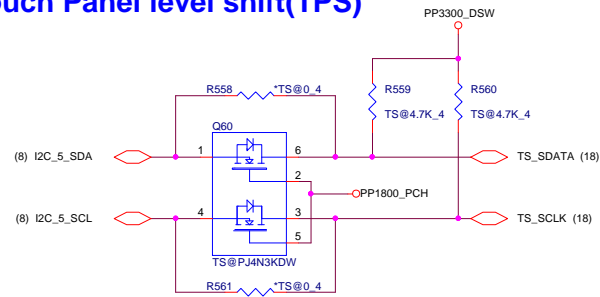
USB OC



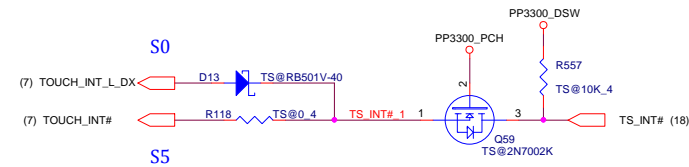
PWRON SEQUENCE



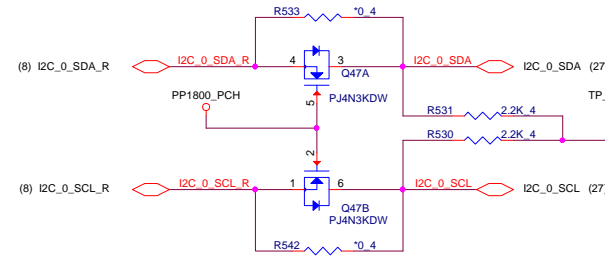
Touch Panel level shift(TPS)



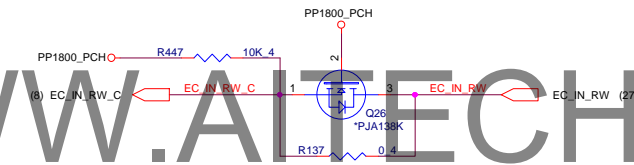
Touch Screen(TPS)



Track Pad

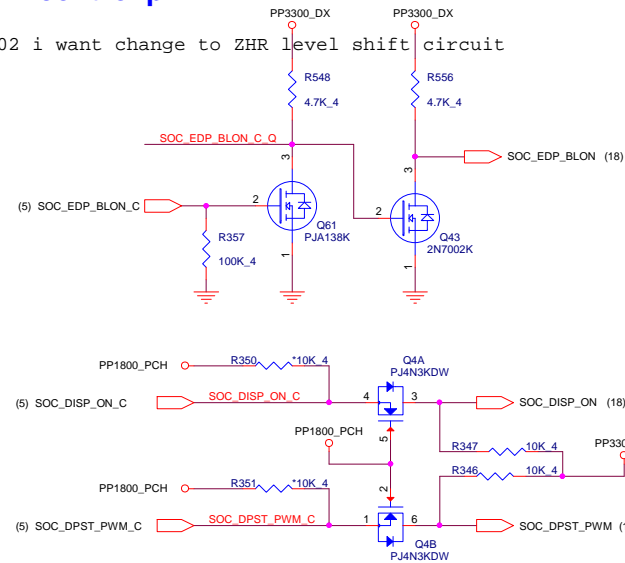


HW RESET

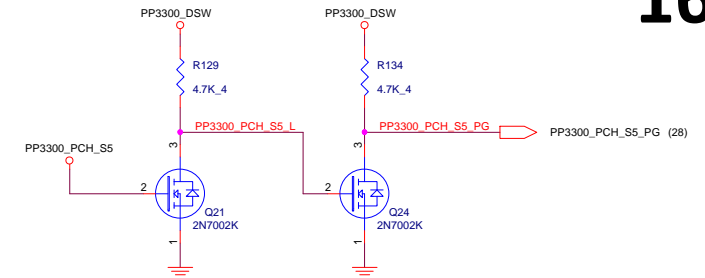


eDP control pin

0402 i want change to ZHR level shift circuit

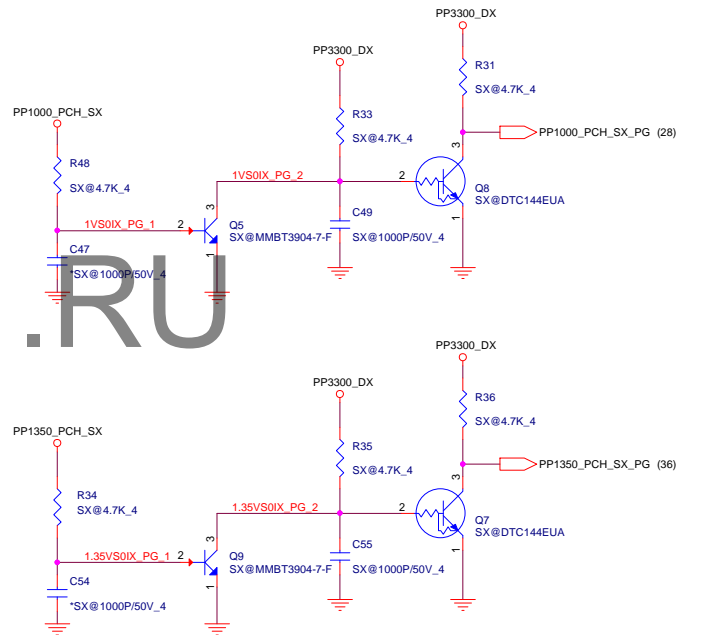


S5 Power Good(+3V_S5)

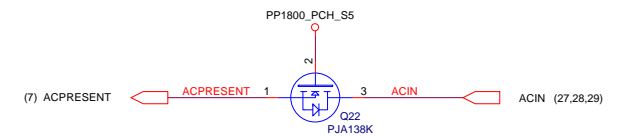


S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed

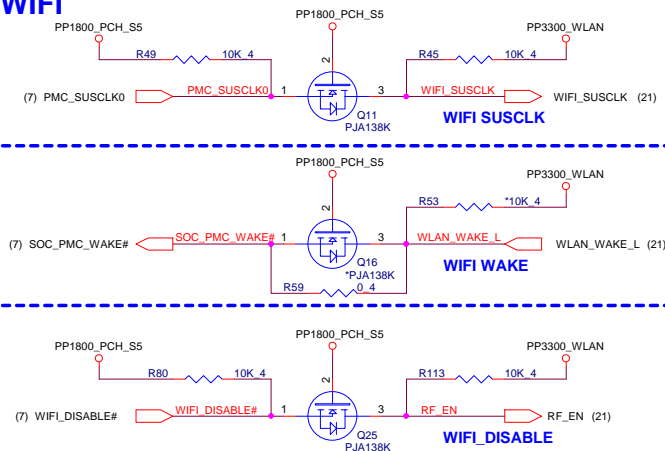


AC Detect



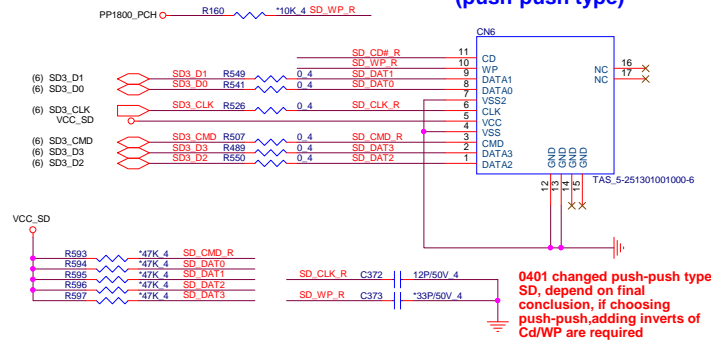
LTE

WIFI

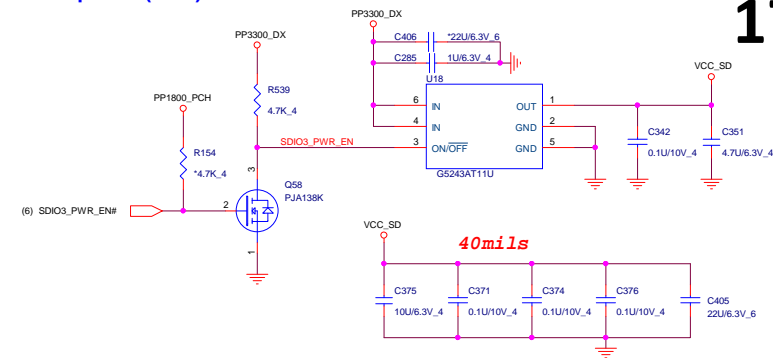


SD/MMC CARD READER CONNECTOR (CBS)

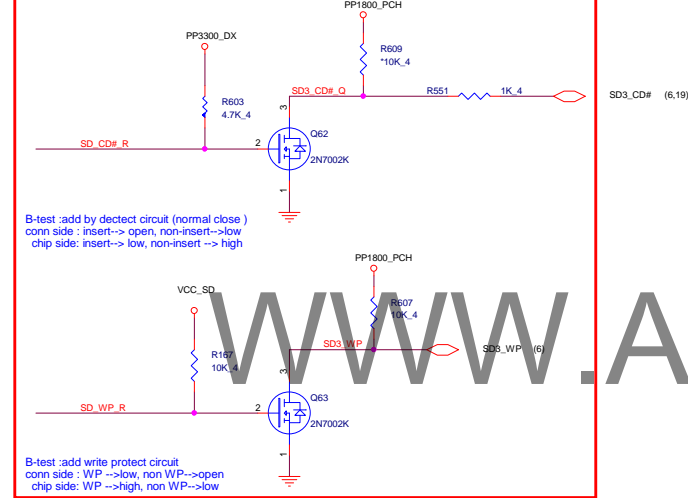
This is full size SD card
(push-push type)



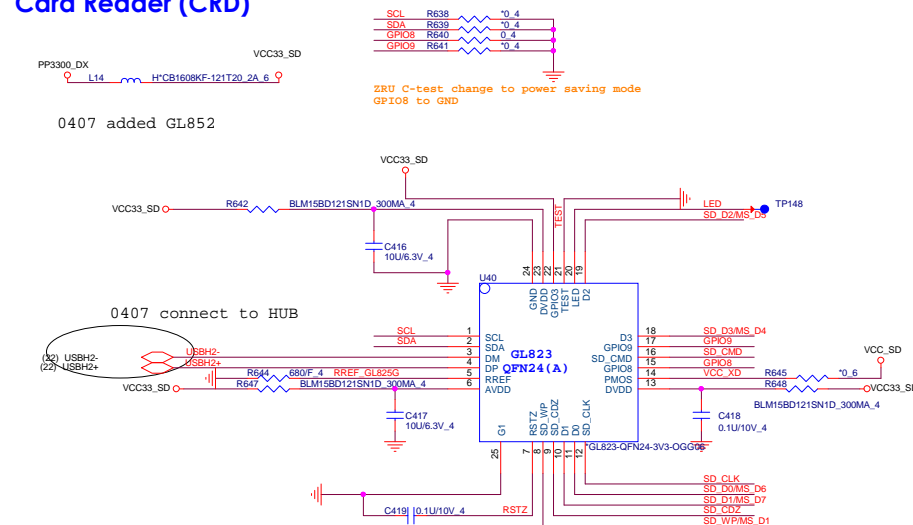
SD card power (CBS)



5/19 change Add CD/WP Reverse



Card Reader (CRD)



GPIO8	GPIO9	FUNCTION
NC	NC	Default Configuration
NC	GND	Remote wake up enable
GND	NC	Power saving enable
GND	GND	ESD mode enable

Application Note

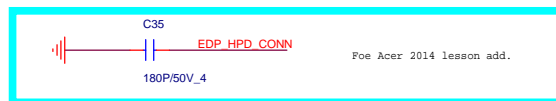
SCL	FUNCTION
NC	Default "Generic STORAGE DEVICE" String
GND	"USB Flash Disk" String

SDA	FUNCTION
NC	Default Support Serial Number
GND	Non Support Serial Number

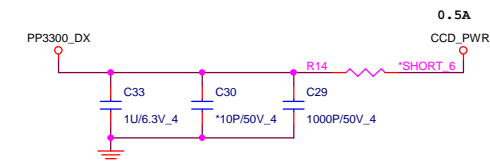
0407 reserved GL852 bus

SD WPMS D1	R643	0.4	SD3 WP
SD CD2	R646	0.4	SD3 CD#
SD D2MS D5	R649	0.4	SD DAT2
SD D7MS D7	R650	0.4	SD DAT1
SD D3MS D6	R651	0.4	SD DAT0
SD CLK	R652	0.4	SD CLK R
SD CMD	R653	0.4	SD CMD R
SD D3MS D4	R654	0.4	SD DAT3

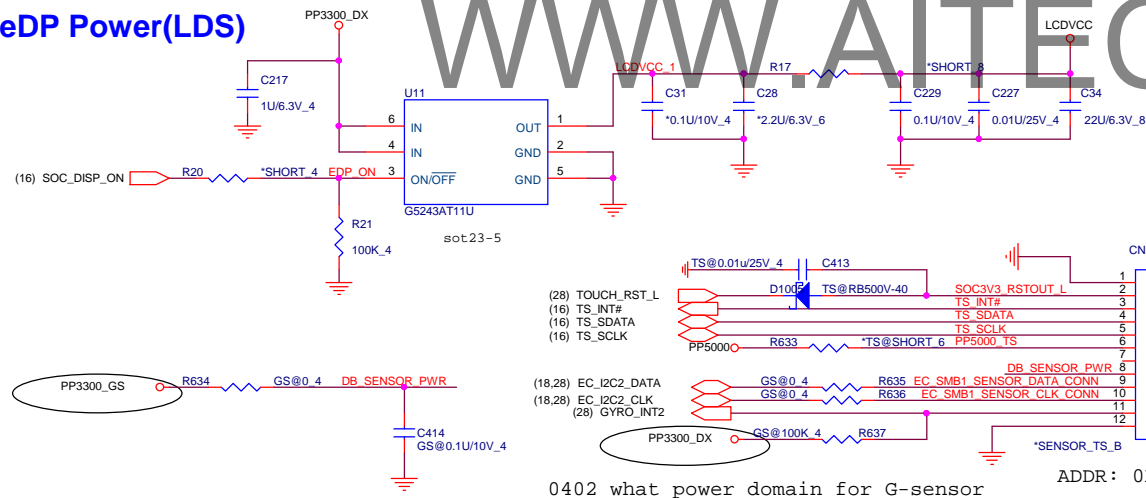
eDP Power(LDS)



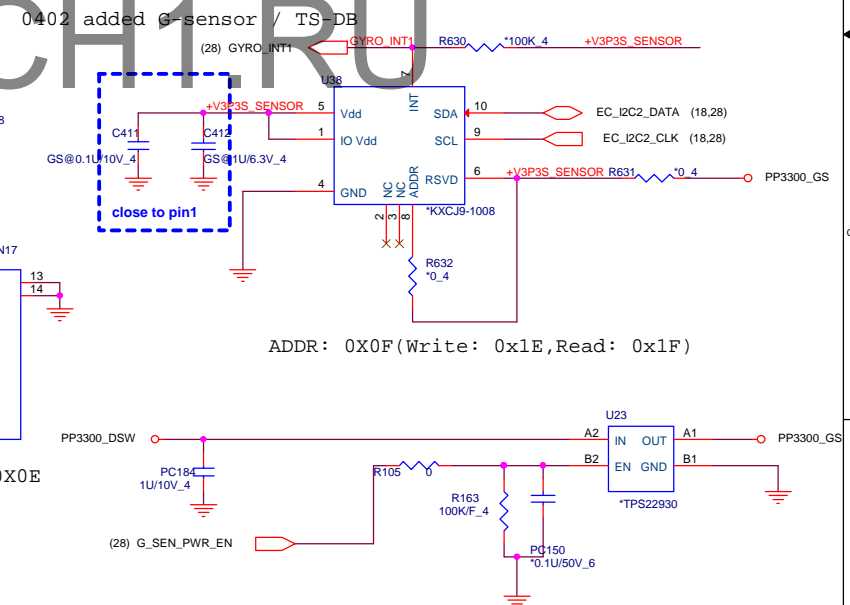
CCD USB(CCD)



eDP Power(LDS)

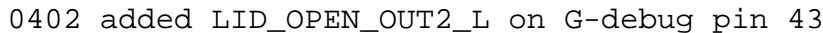


0402 what power domain for G-sensor

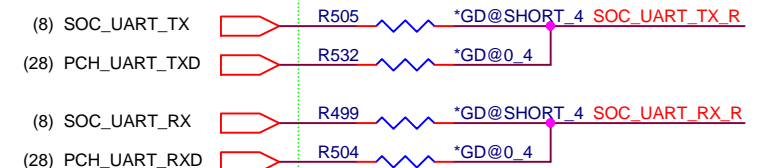


19

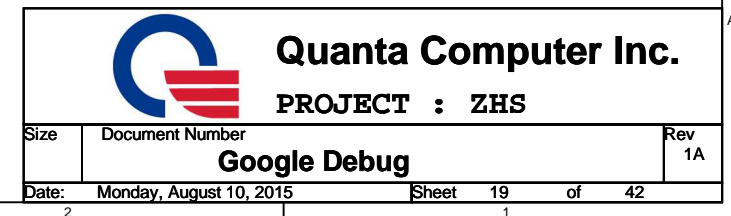
PIN7	OD	PIN39	OD	PIN49	OD
PIN14	OD	PIN41	OD	PIN50	OD
PIN19	OD	PIN43	OD		
PIN22	OD	PIN44	OD		
PIN28	OD	PIN45	OD		
PIN30	OD	PIN46	OD		
PIN37	OD	PIN47	OD		
PIN38	OD	PIN48	OD		



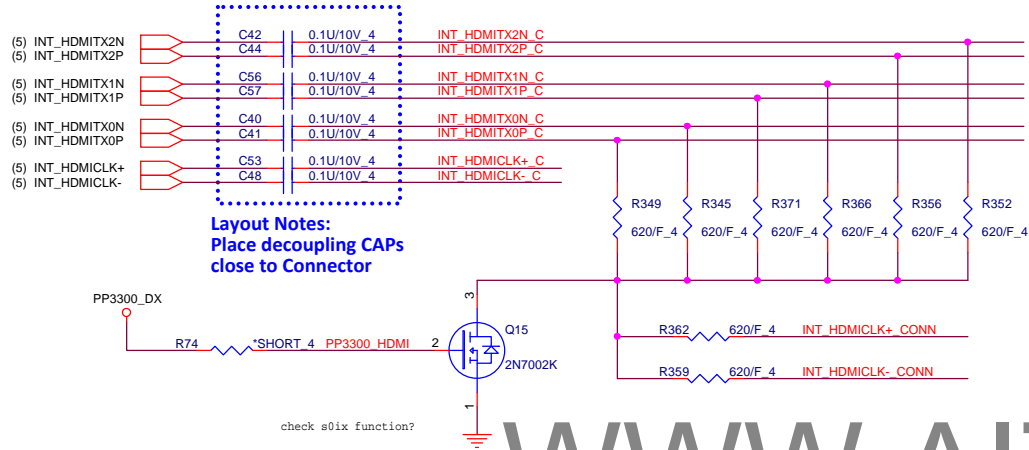
UART(MPC)



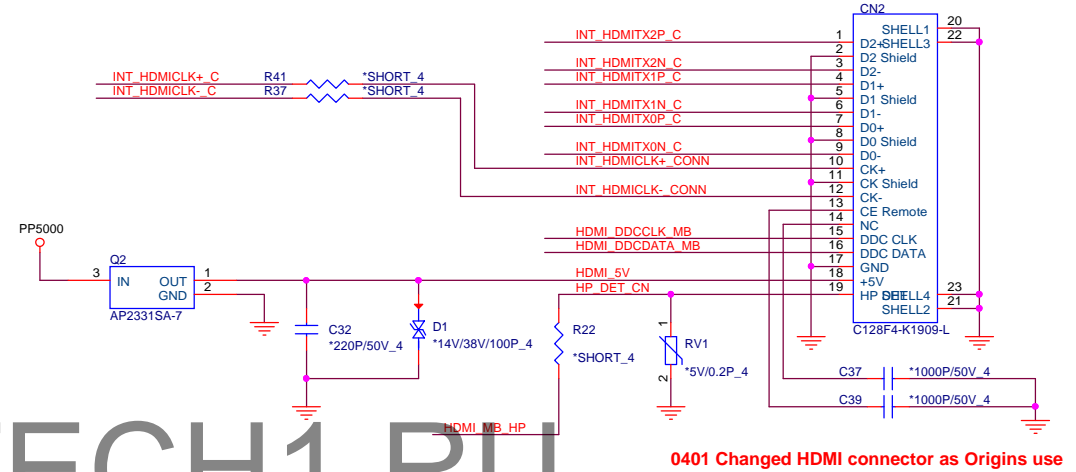
UART option from SOC/PCH



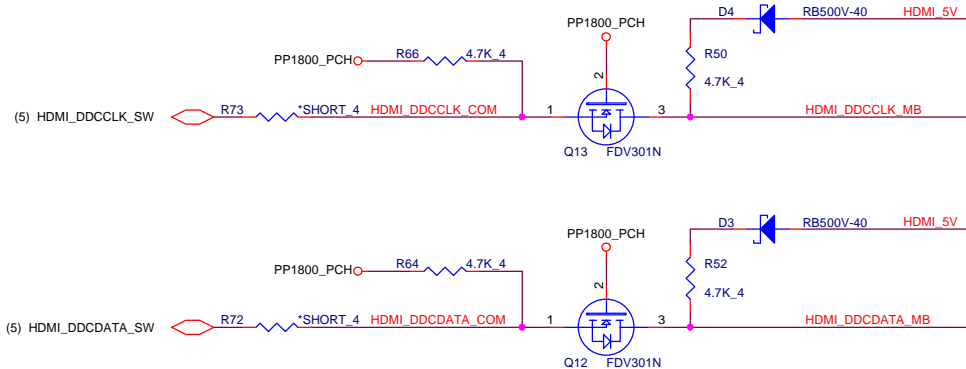
HDMI Cost Reduced level shift (HDM)



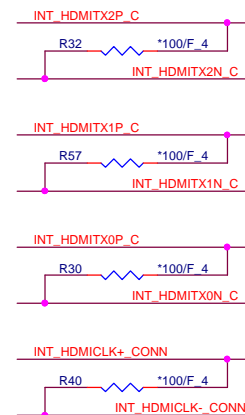
HDMI connector (HDM)



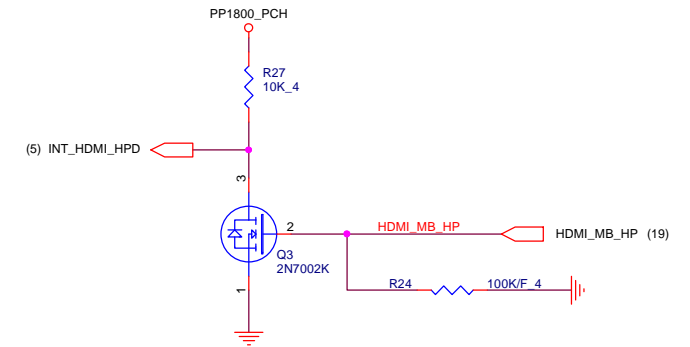
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



WIFI/BT COMBO NGFF E KEY(MNC)

21

(Low Active)
(Low Active)

WLAN_OFF_L POWER DOWN LAN CHIP from EC?
WIFI_DISABLE_L disable Antenna from PCH?

(16) RF_EN
(28) WLAN_OFF_L
(15,23,28) PLTRST#
(16) WIFI_SUSCLK

TP27
TP26
TP25

NFC_ANT_N
NFC_ANT_P
NFC_VDDANT

PIN54: disable Antenna
PIN52: power down CHIP

RF_EN
PDN#
WLAN_RST#

TP42
TP43

LTE_SOUT
LTE_SIN

TP29
TP1
TP39

NFC_WI_IN
NFC_SWP2_IO
NFC_ACTIVE

NFC Security
WIFI_UART_RX

+WL_VDD

R47 *10K_4 PDN#

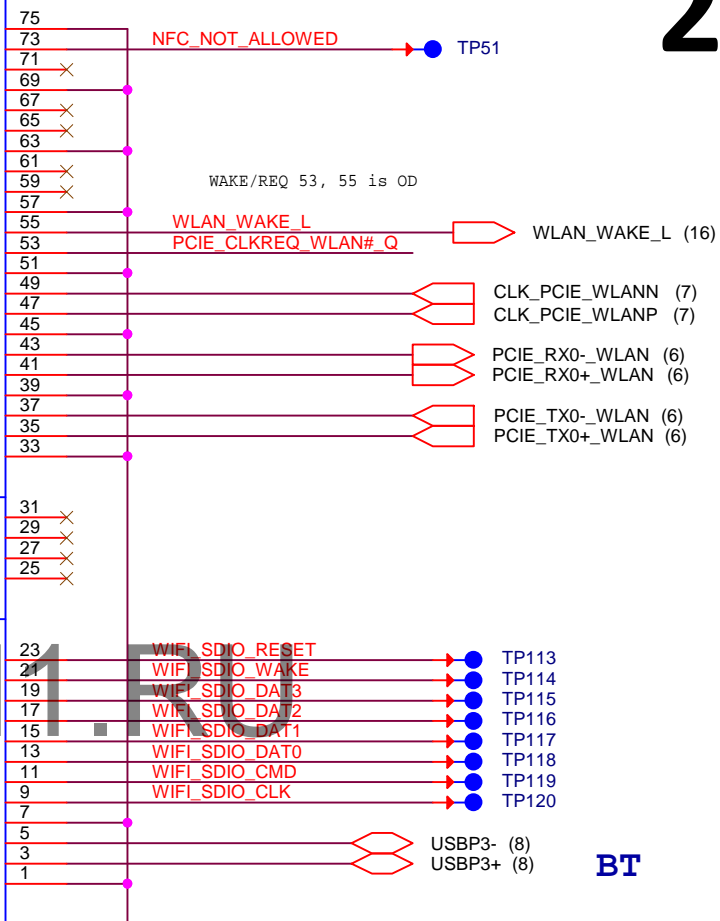
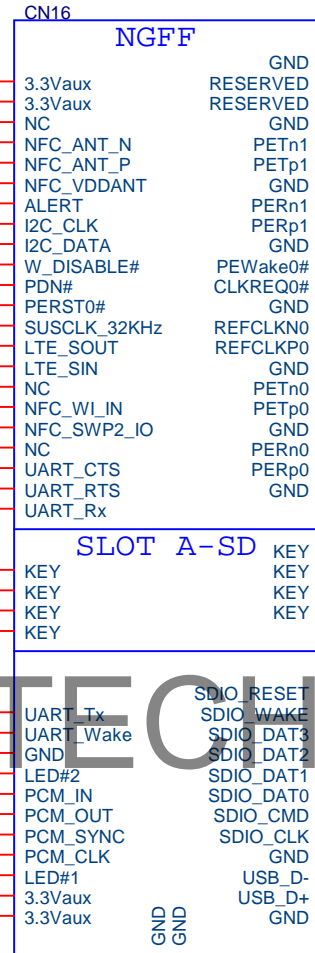
TP30
TP3

WIFI_UART_TX
BT_LED

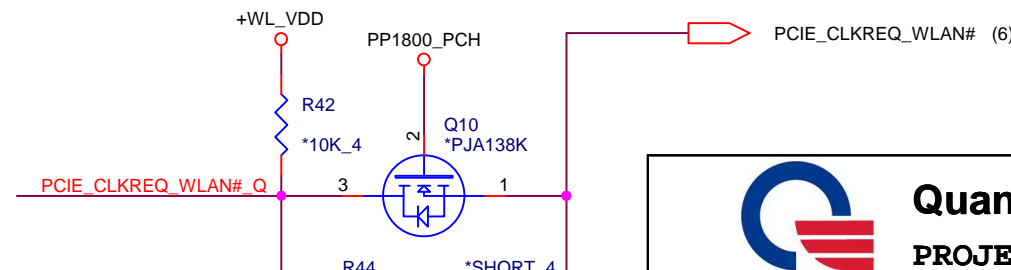
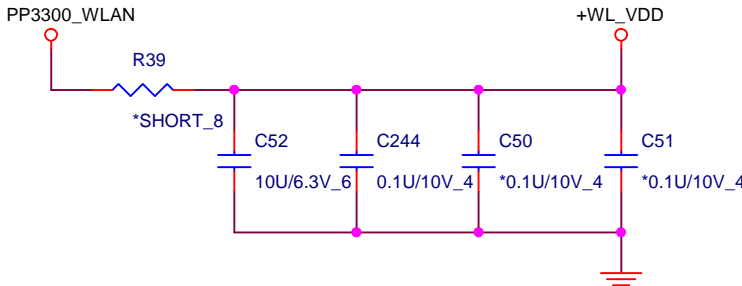
TP129
TP130
TP131
TP132
TP2

PCM_IN
PCM_OUT
PCM_SYNC
PCM_CLK
WLAN_LED1#

+WL_VDD



WL/BT NGFF Power



0401 Changed WiFi NGFF connector as Origins use



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PROJECT : ZHS

H



B

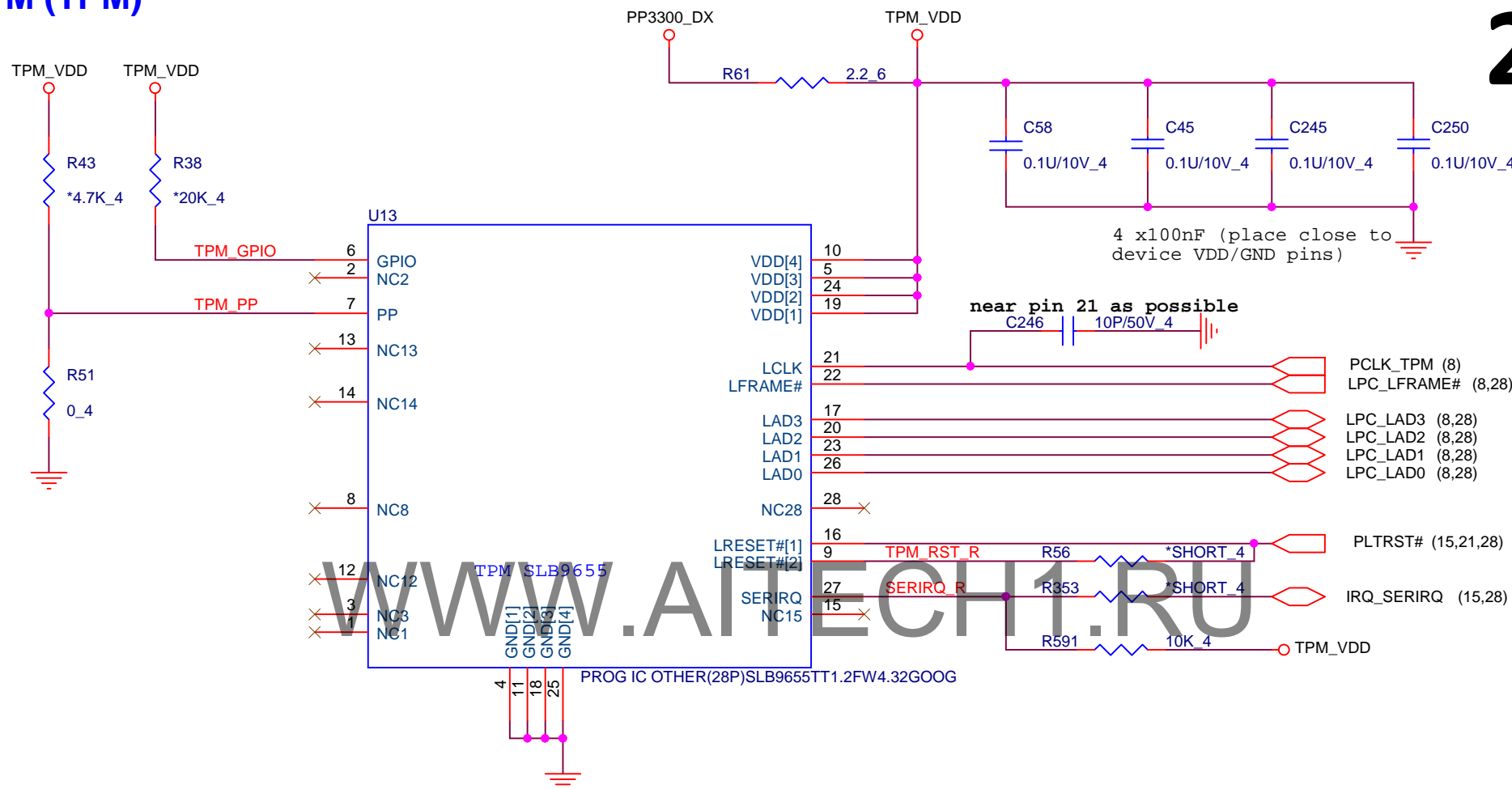


A



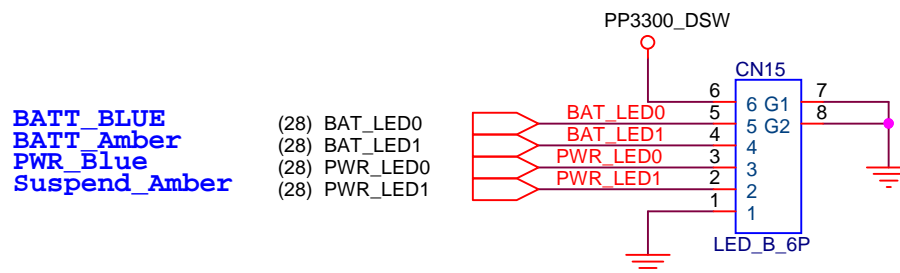
TPM (TPM)

23



LED board(UIF)

0402 Changed LED board connector as Origins use

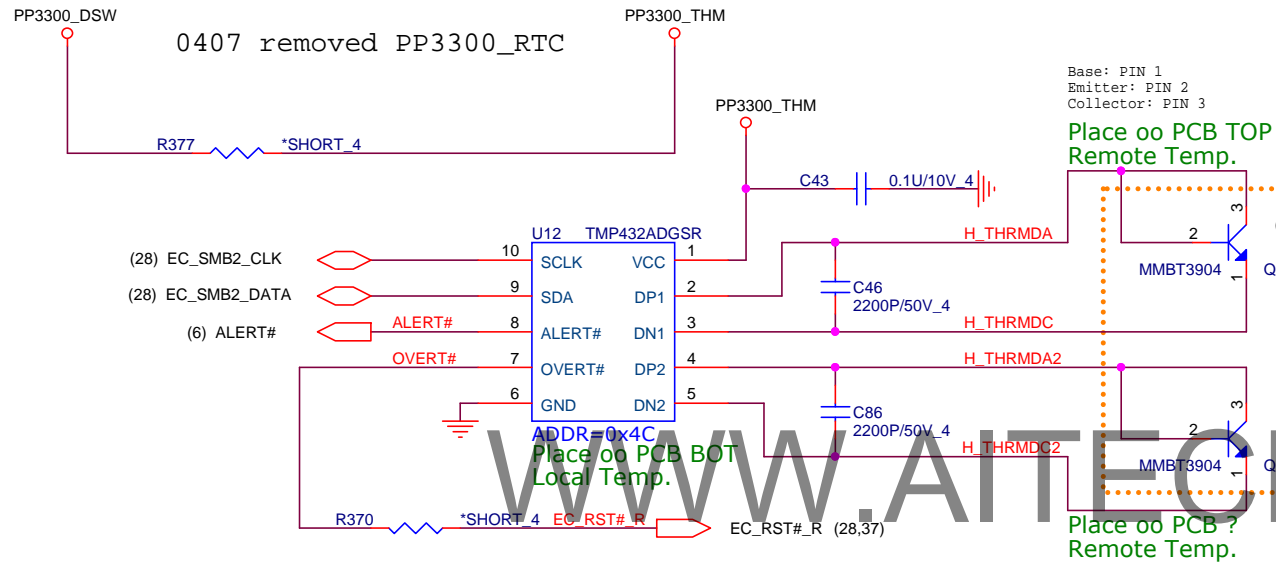


Quanta Computer Inc.

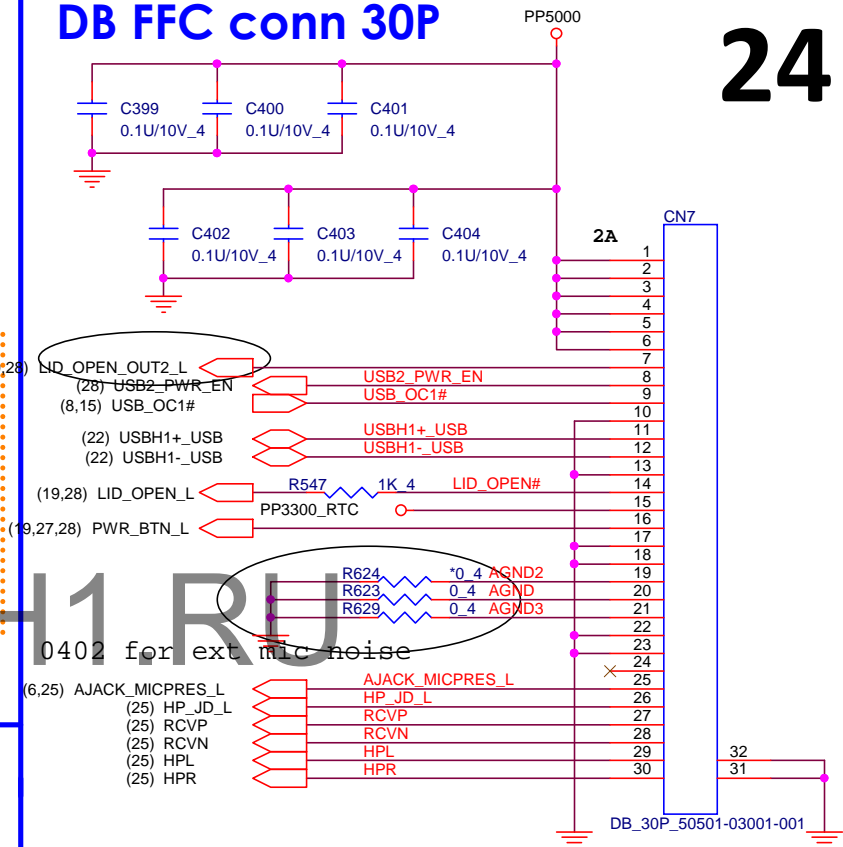
PROJECT : ZHS

Size	Document Number	Rev
	TPM SLB9655 / LED	1A
Date:	Monday, August 10, 2015	Sheet 23 of 42

Thermal Sensor(THM)

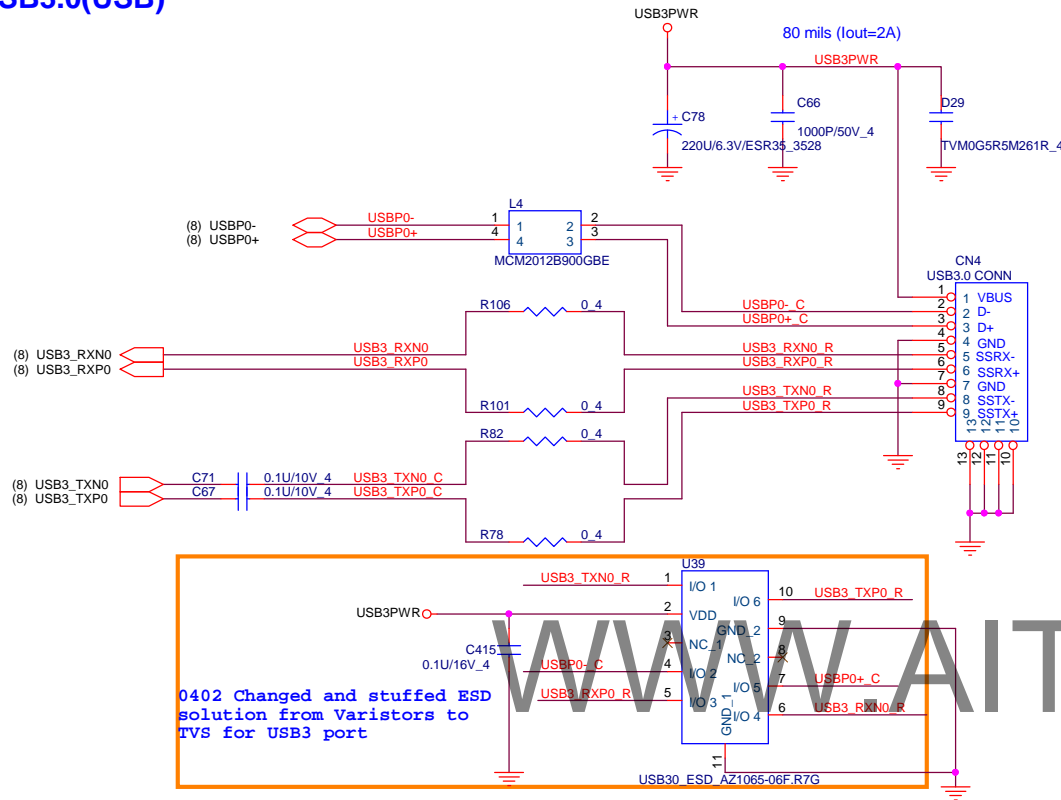


DB FFC conn 30P

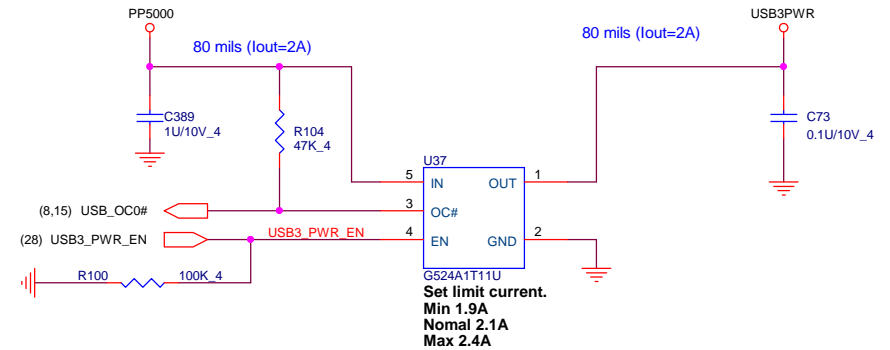


USB 2.0_ILIM_SEL (USB)

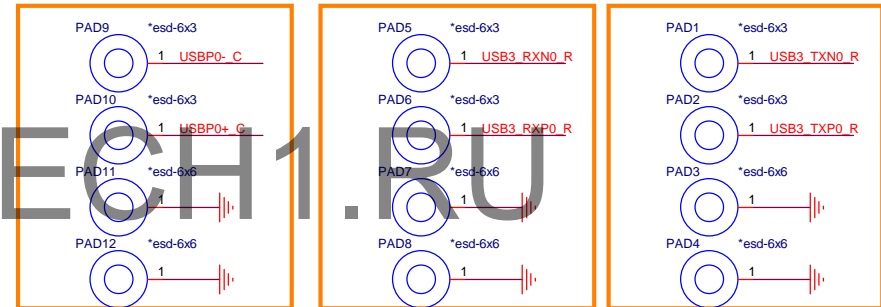
USB3.0(USB)



USB Switch

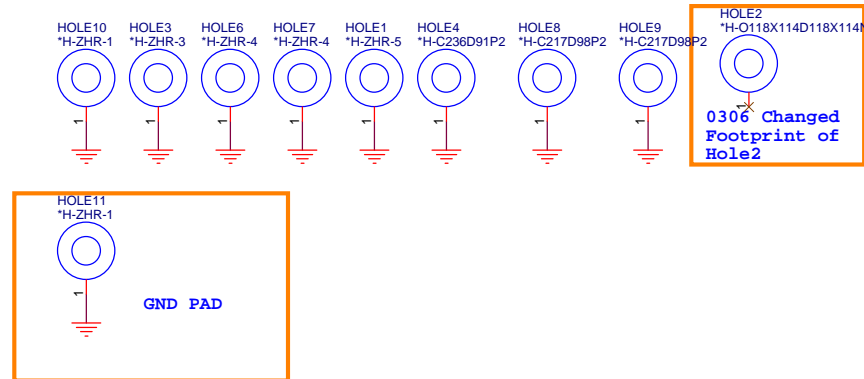
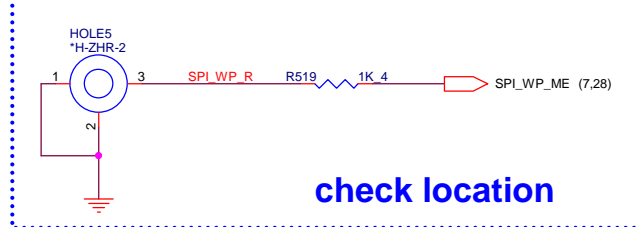


0804 Added PAD1-12
as ESD protection



HOLE(OTH)

ROM WP#

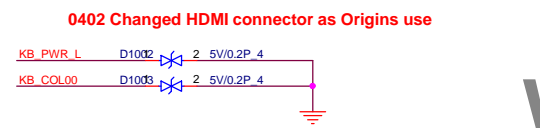
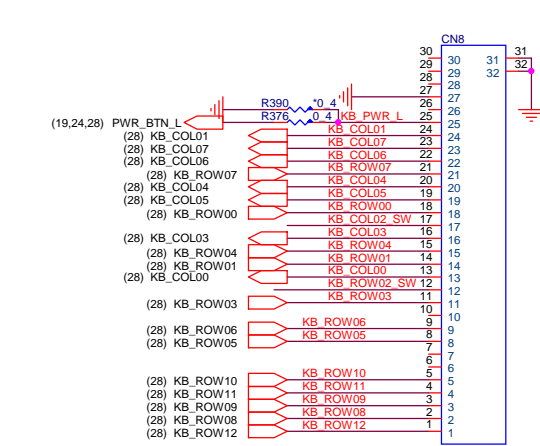


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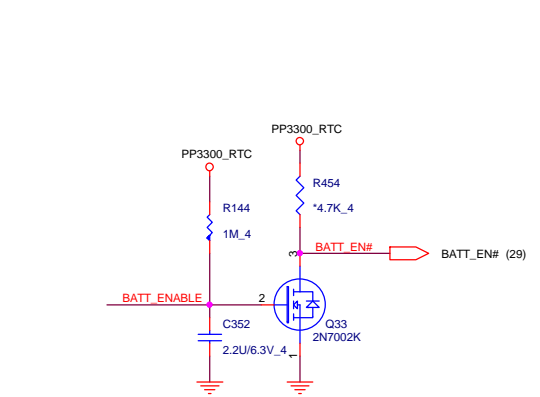
PROJECT : ZHS

Size	Document Number	Rev
	USB3/Hole	1A
Date:	Monday, August 10, 2015	Sheet 26 of 42

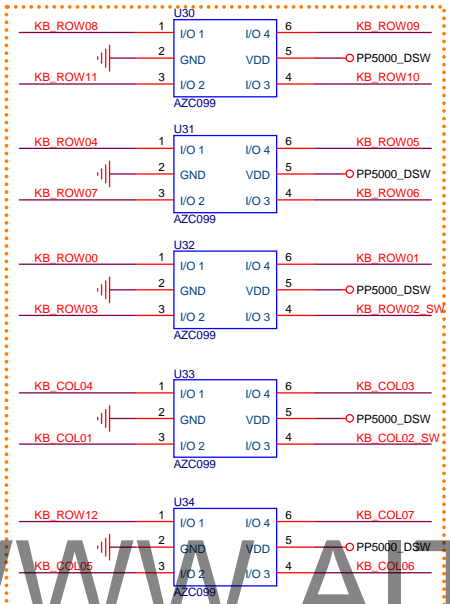
K/B (KBC)



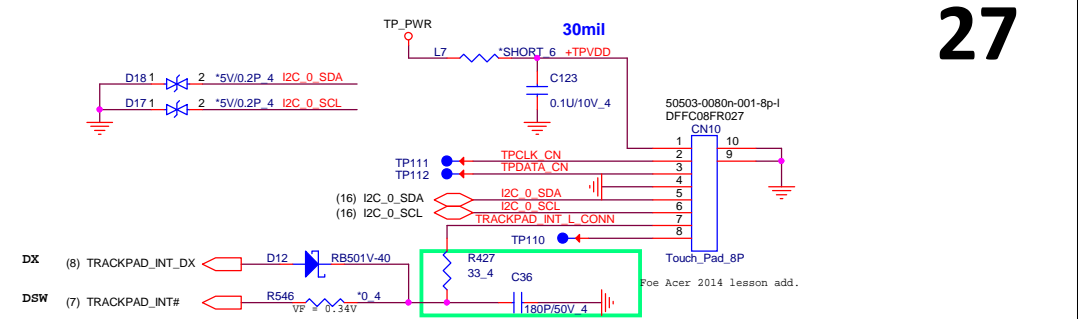
HOLELESS RESET 2-CHIP(KBC)



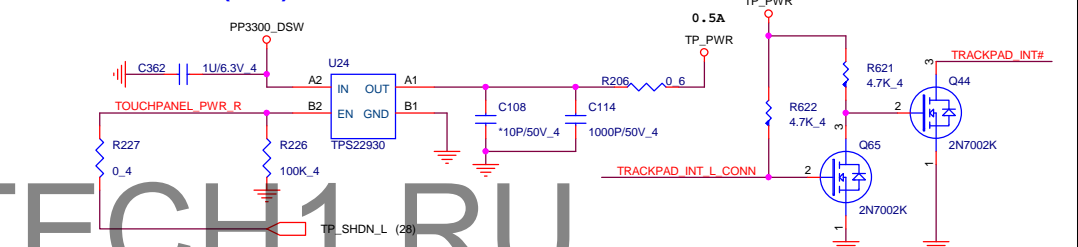
0407 removed SW1



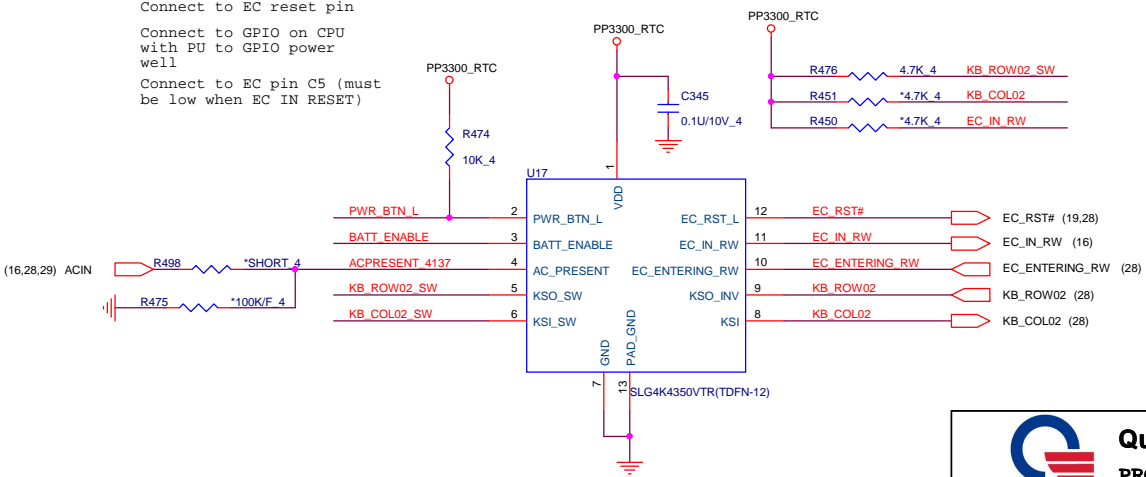
Track PAD BOARD CONN (TPD)

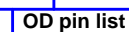


Track PAD Power(TPD)



Connect to EC reset pin
Connect to GPIO on CPU
with PU to GPIO power
well
Connect to EC pin C5 (must
be low when EC IN RESET)

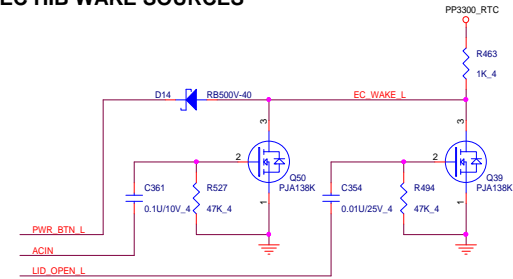
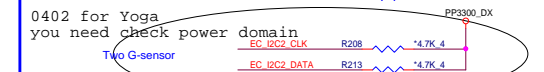
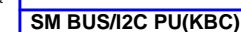




For testing only



Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1
Date:	Monday, August 10, 2015	Sheet 28 of 42



SM BUS ARRANGEMENT TABLE

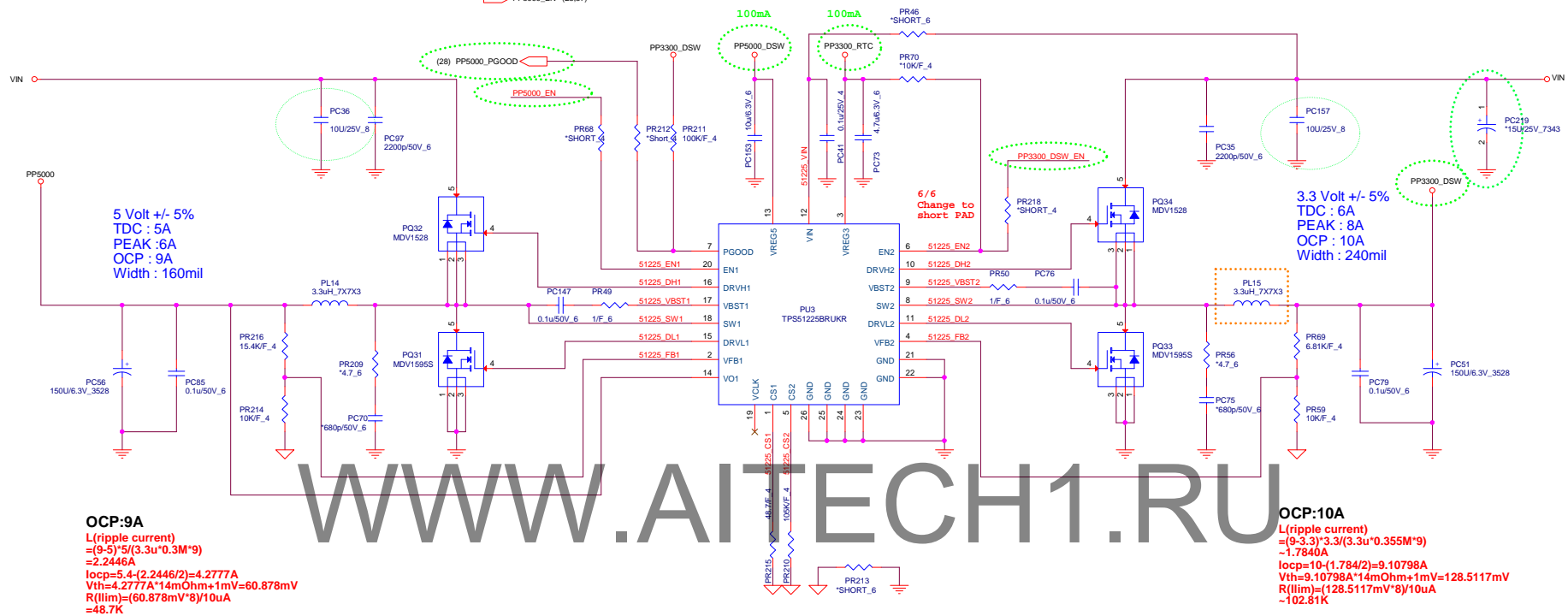
SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR
I2C2	Two G-sensor

Battery cell select

3 Cell	float
4 Cell	High

PP3300_EC

 Battery Cell Sw (29)



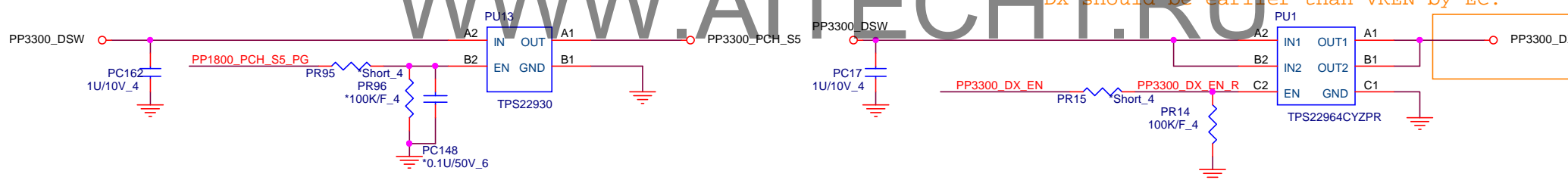
$L(\text{ripple current}) = (9-5) \cdot 5 / (3.3 \cdot 0.3 \cdot 9) = 2.2446 \text{ A}$
 $I_{\text{ocp}} = 5.4 - (2.2446 / 2) = 4.2777 \text{ A}$
 $V_{\text{th}} = 4.2777 \text{ A} \cdot 14 \text{ m}\Omega + 1 \text{ mV} = 60.878 \text{ mV}$
 $R(I_{\text{lim}}) = (60.878 \text{ mV} \cdot 8) / 10 \mu\text{A} = 48.7 \text{ k}\Omega$

$L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (3.3\mu \cdot 0.355\text{M}^9)$
 $\sim 1.7840\text{A}$
 $I_{\text{ocp}} = 10 - (1.784/2) = 9.10798\text{A}$
 $V_{\text{th}} = 9.10798\text{A} \cdot 14\text{m}\Omega + 1\text{mV} = 128.5117\text{mV}$
 $R(\text{Ilim}) = (128.5117\text{mV}^8) / 10\mu\text{A}$
 $\sim 102.81\text{k}$



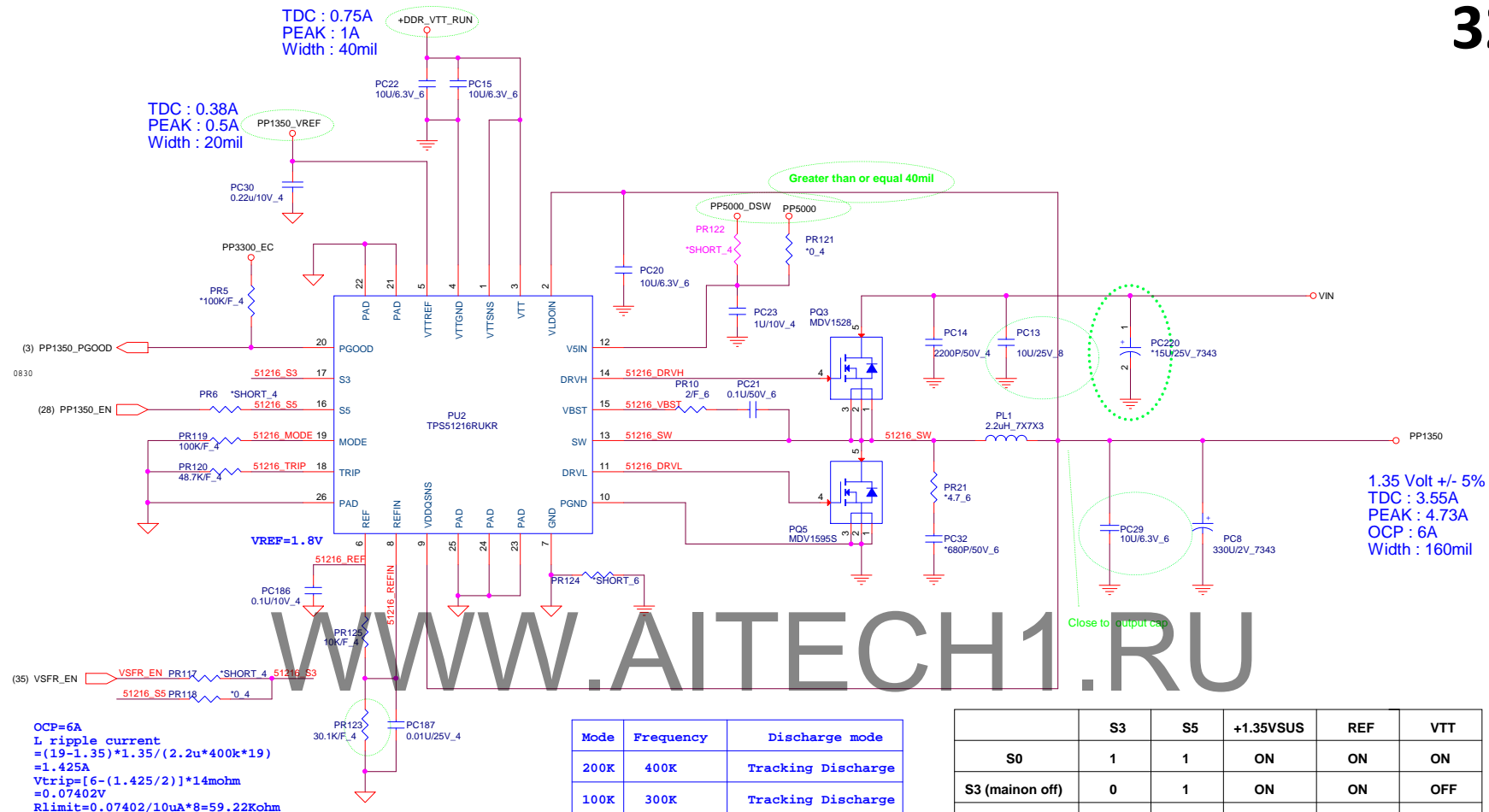
WWW.AITECH1.RU

DX should be earlier than VREN by EC.



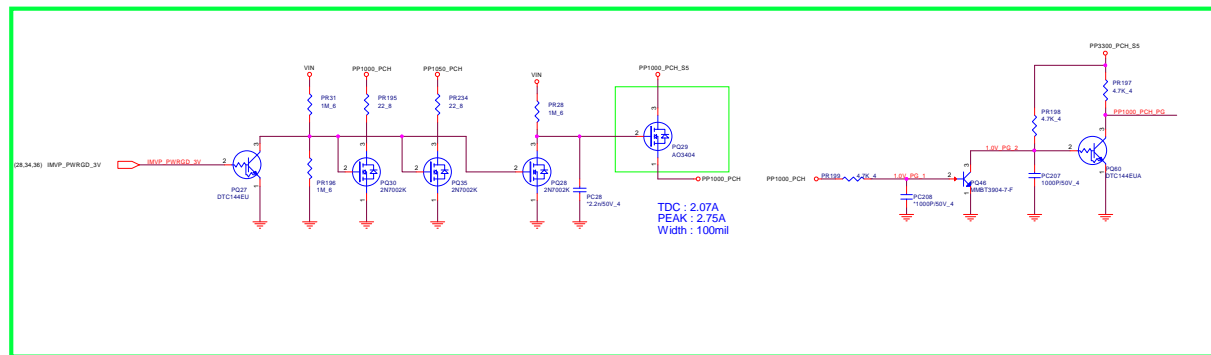
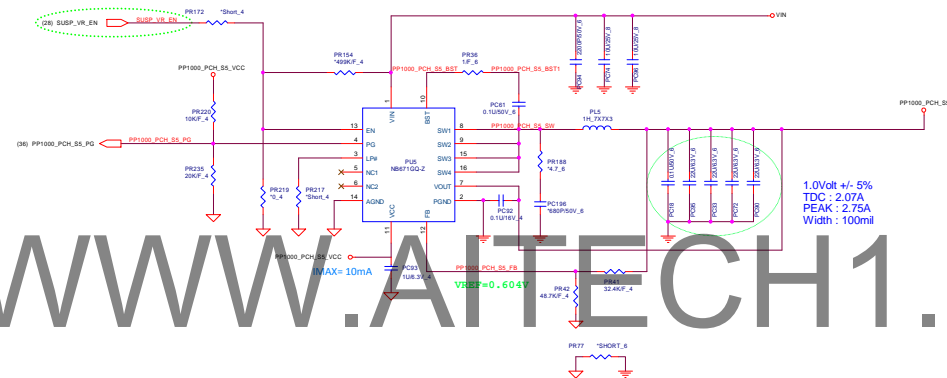
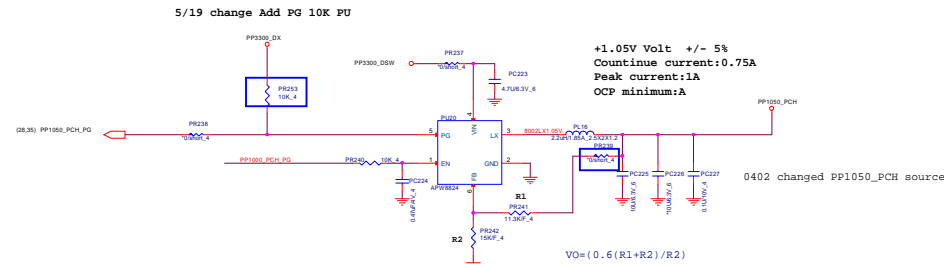
PROJECT :

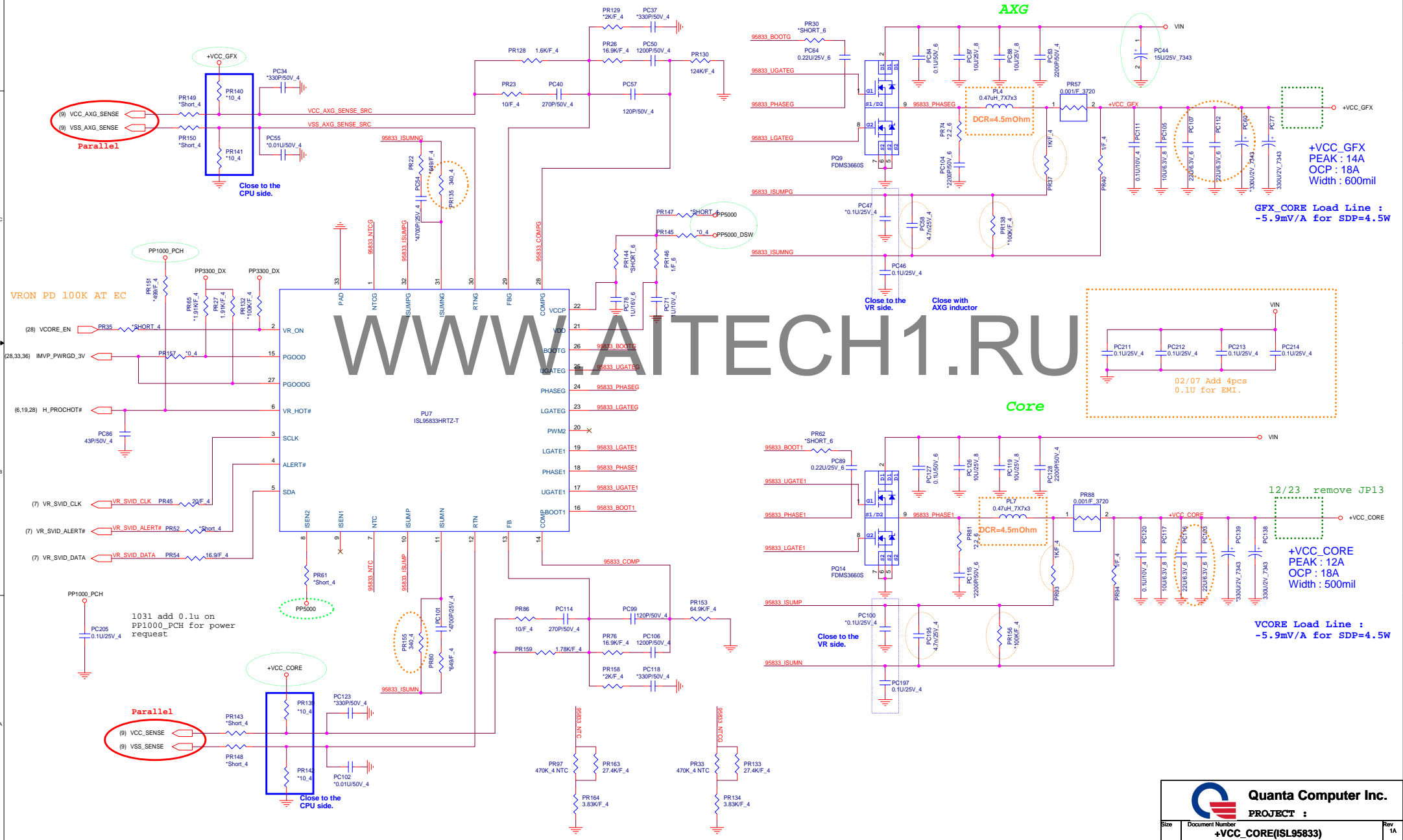
Size	Document Number Load Switch	Rev 1A
Date:	Monday, August 10, 2015	Sheet 31 of 42



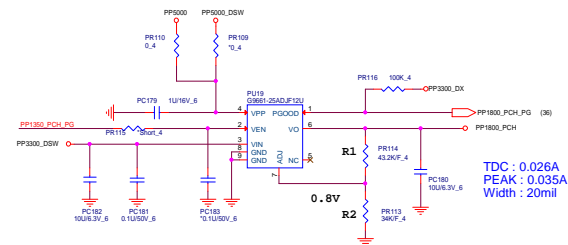
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PROJECT :

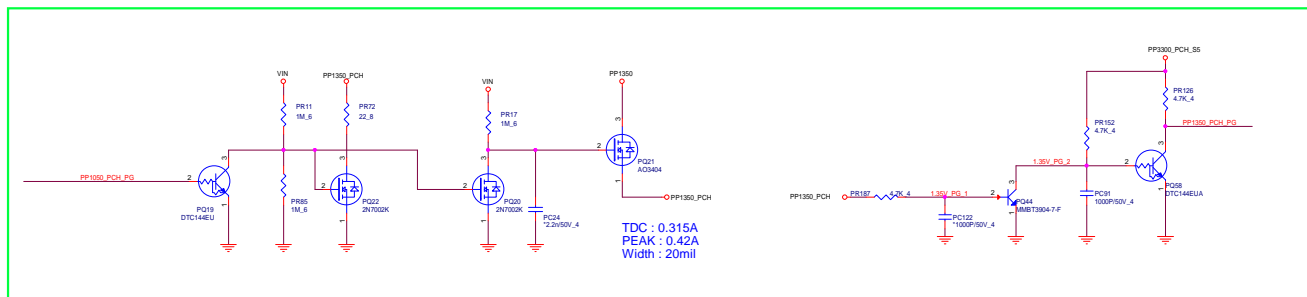
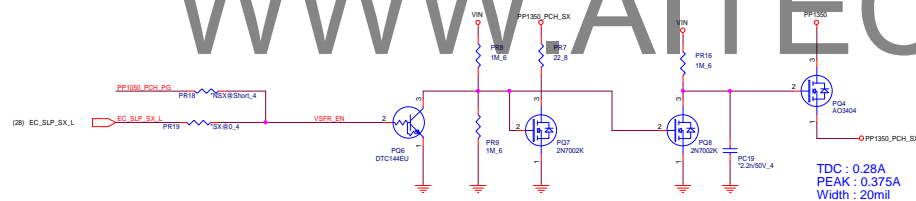




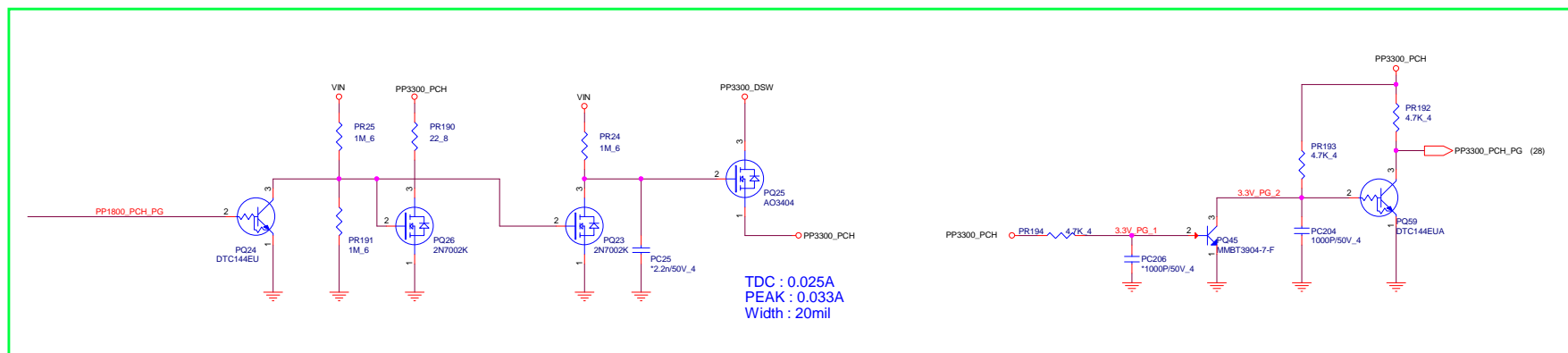
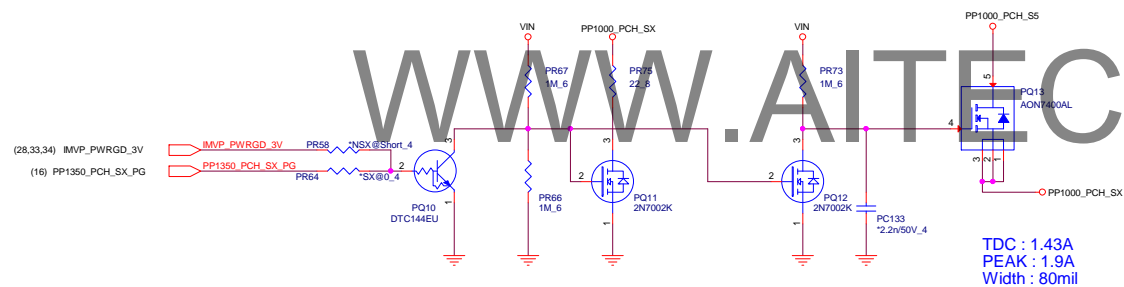
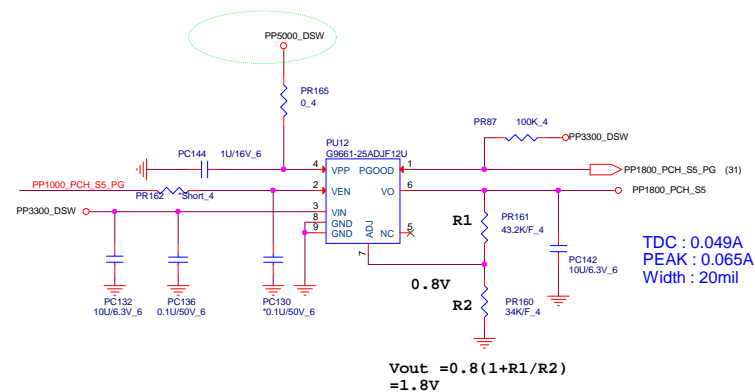
(32) VSFR_EN
(28,33) SUSP_VR_EN
(28,33) PP1050_PCH_PG



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(35) PP1800_PCH_PG
(33) PP1000_PCH_S5_PG



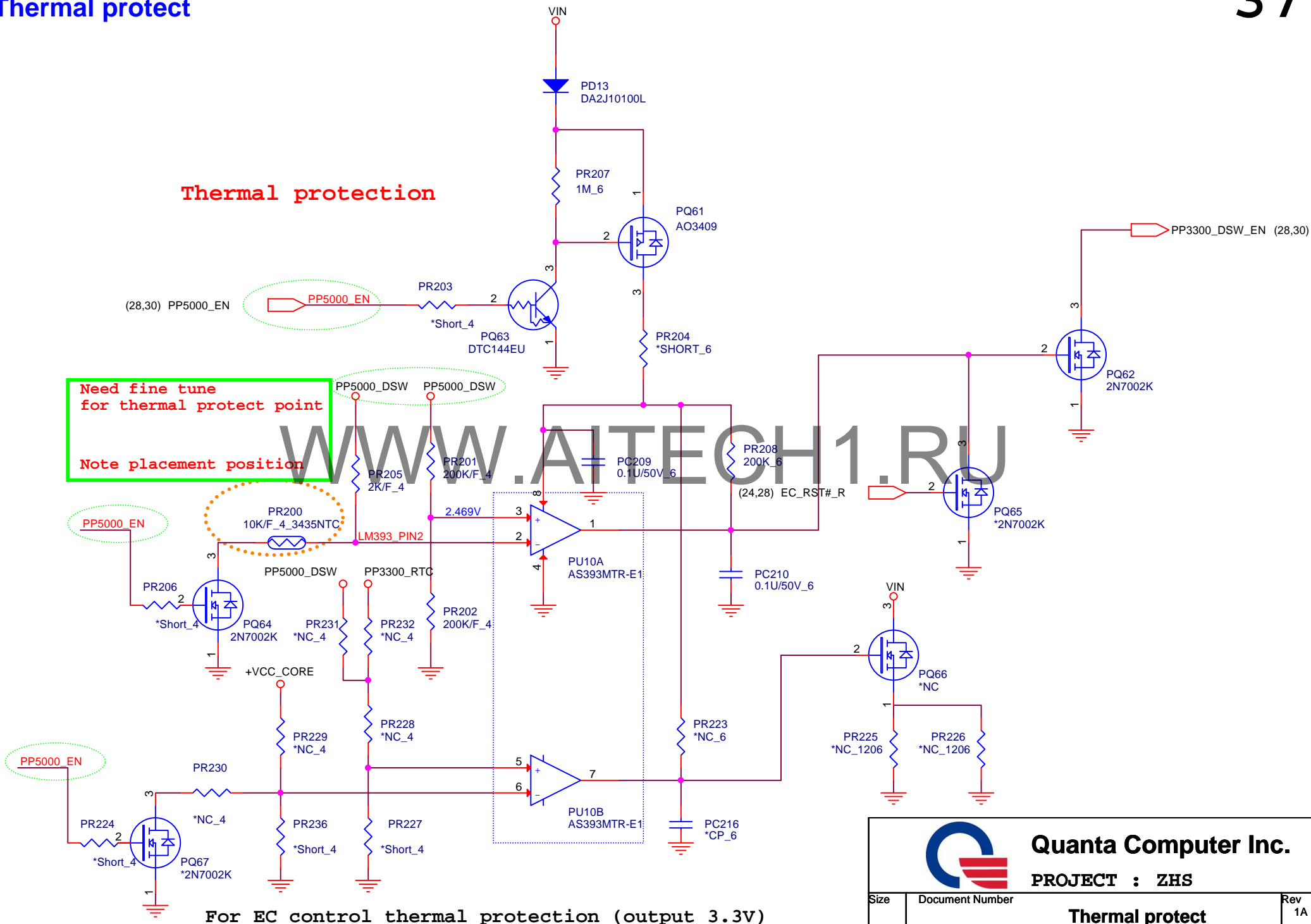
Thermal protect

37

Thermal protection

Need fine tune
for thermal protect point

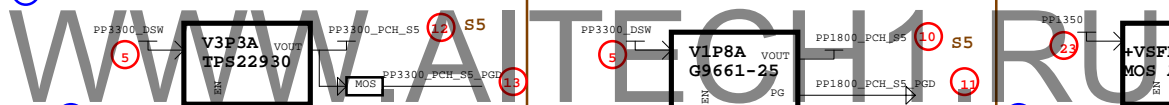
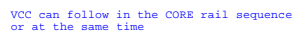
Note placement position



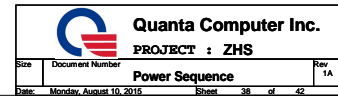
Quanta Computer Inc.

PROJECT : ZHS

Size	Document Number	Thermal protect	Rev 1A
Date:	Monday, August 10, 2015	Sheet 37 of 42	



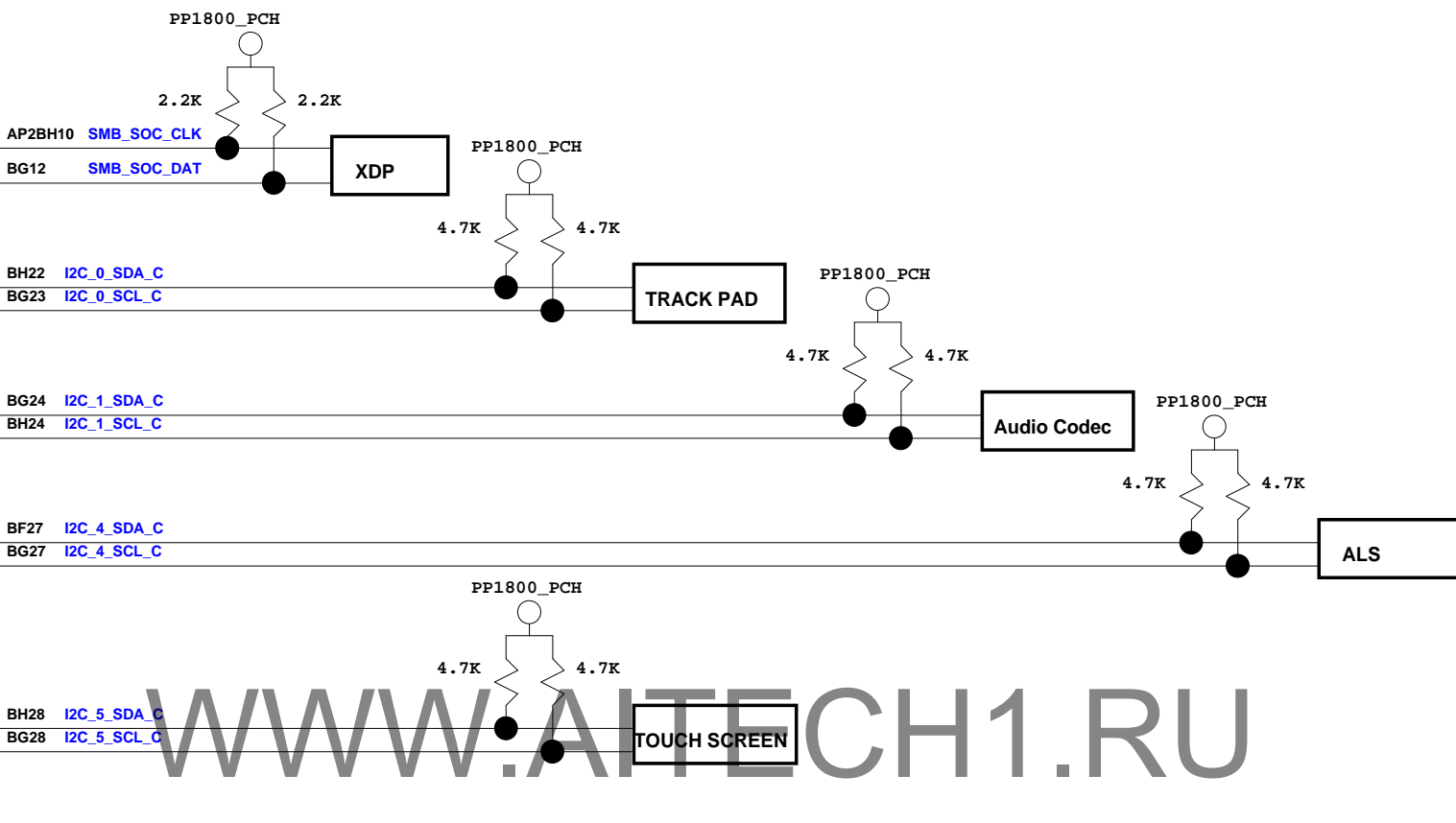
a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling



SMBUS

Bay-trail M

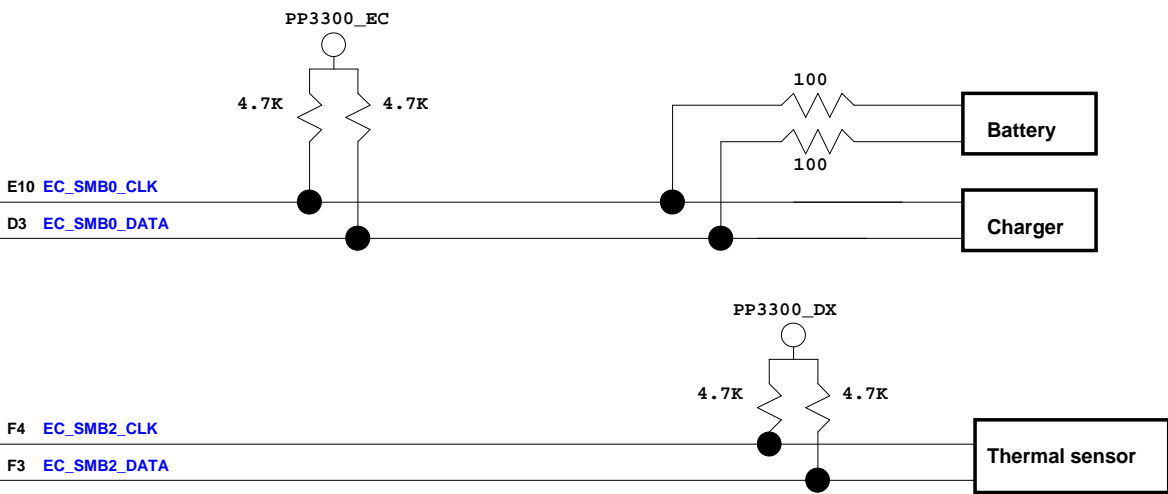
I2C

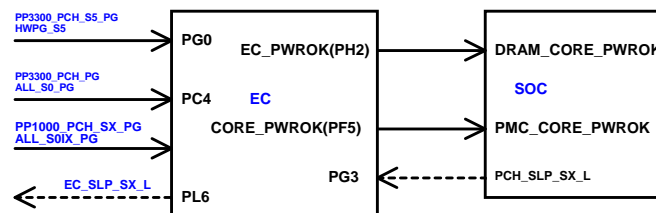
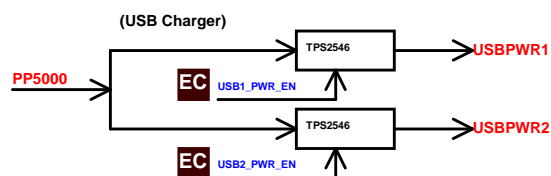
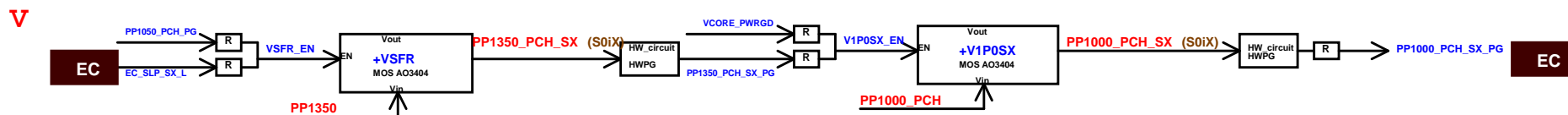
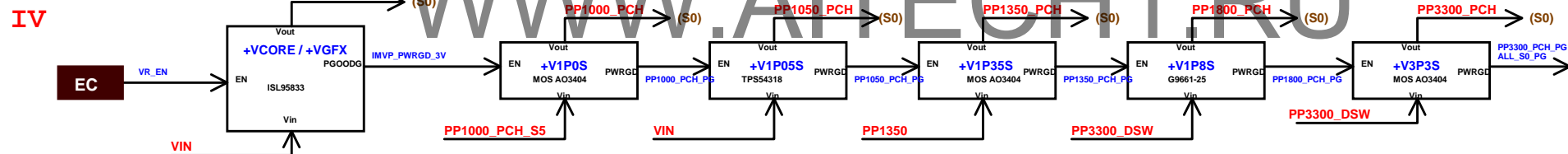
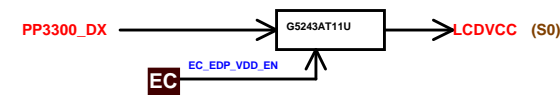
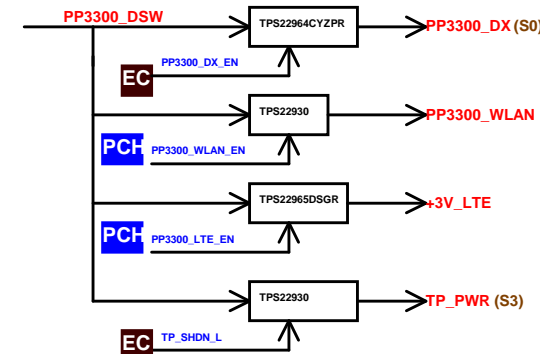


KBC

TI

SMBUS





Model	Version	CHANGE LIST
ZHS M/B	1A	<p>1. 2015/05/19 :Update RAM ID for ZHQ and ZHS use.(page8)</p> <p>2. 2015/05/19 : add R200 and R214 LTE_WAKE# and PMC_SUSCLK1 pull high to PP1800_PCH_S5 for can't into S3 issue (Page7)</p> <p>3. 2015/05/19 : add R426 LTE_DISABLE# Pull-High to PP1800_PCH_S5 for can't into S3 issue.(Page 8)</p> <p>4. 2015/05/19 : add R603/R609/Q62/R167/R607/Q63 FOR SD Card can't work issue.(page 17)</p> <p>5. 2015/05/19 : add PR523 10k Pull-high to PP3300_DX for can't power on issue (Page 41)</p> <p>6. 2015/05/19 : add PR234 and PQ35 for PP1050_PCH 放電線路 (Page 41)</p> <p>7. 2015/05/19 : EMI request add PC189 for EMI issue. (Page 39)</p> <p>8. 2015/05/19 : EMI request add C112 for EMI issue. (page22)</p> <p>9. 2015/05/19 : EMI request add C130/C132 DMIC CLK/DAT for EMI issue (Page22)</p>
		<p>1. 2015/06/19 : Add C35 and Change R326 to 33 ohm for Acer ESD request (page18)</p> <p>2. 2015/06/19 : Add Pad1-Pad12 for Acer ESD request (page26)</p> <p>3. 2015/06/19 : Add R427 33 ohm Acer ESD request (page27)</p> <p>4. 2015/06/19 : Del R490 , Add R516 for SANYO battery</p> <p>5. 2015/06/19 : Change 0 ohm to Short Pad: R14,R17,R39,R217</p> <p>6. 2015/08/10 : Change 0 ohm to Short Pad: PR46,PR218,PR68,PR248,PR244,PR247,PR243,PR249,PR245,PR122,PR6,PR117,PR250,PR246</p>

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DOC NO.	PROJECT MODEL	Chrome	APPROVED BY:	DATE:	
	PART NUMBER:		DRAWING BY:	REVISION:	

Quanta Computer Inc.

PROJECT : 828

Change list

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Model		Version	CHANGE LIST				41
	2B						
	3C						
	3D						
DOC NO.	PROJECT MODEL	Chrome	APPROVED BY:	DATE:			 Quanta Computer Inc. PROJECT : 848 Change list
	PART NUMBER:		DRAWING BY:	REVISION:			